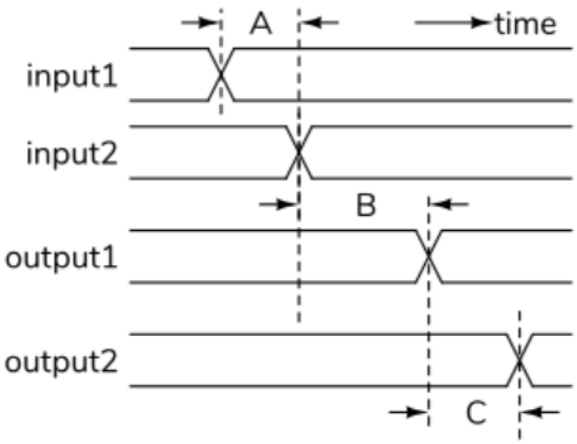
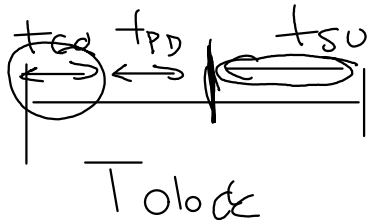
Timing Analysis

Exercise 1: Label the specifications A through C as requirements or guaranteed responses.



	measured to	
A	input2	requirement
B	output 1	guaranteed response
C	output 2	guaranteed response

Exercise 2: Which of the specifications in the formula above decrease the available setup time as they increase? Which increase it?



$$t_{SU} = T_{clock} - t_{CO} - t_{PD}$$

decreases t_{su}

decreases t_{su}

increases t_{su}

} avail.

Exercise 3: For a particular circuit f_{clock} is 50 MHz, t_{CO} is 2 ns (maximum), the worst-case (maximum) t_{PD} in a circuit is 15 ns and the minimum setup time requirement is 5 ns. What is the setup time slack? Will this circuit operate reliably? If not, what it the maximum clock frequency at which it will?

$f_{clock} = 50\text{MHz}$ $\quad T_{clock} = \frac{1}{f_{clock}} = \frac{1}{50\times10^6} = 20\text{ ns}$

$t_{PD} = 15\text{ ns}$

$t_{co} = 5$ $\quad t_{su(avail)} = T_{clock} - t_{PD} - t_{co}$

$= 20 - 15 - 2 = 3\text{ ns}$

$\text{slack} = t_{su(avail)} - t_{s(reqd)} = 3 - 5 = -2\text{ ns}$

No, will not work reliably.

need $t_{su(avail)} = 5\text{ ns}$.

$\rightarrow 5 = T_{clock} - 15 - 2$

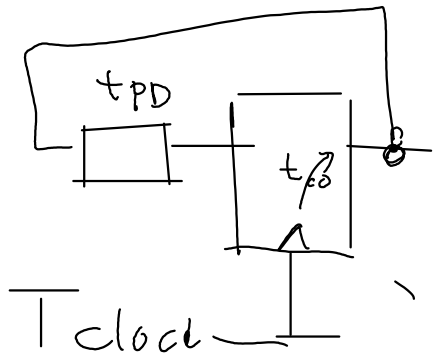
$T_{clock} = 5 + 15 + 2 = 22\text{ ns}.$

$f_{clock} = \frac{1}{T_{clock}} = 45\text{ MHz}$

Exercise 4: What is the maximum clock frequency for a counter using flip-flops with 200 ps setup times, 50 ps hold times and adder logic that has a 250 ps propagation delay?

t_{co}

$t_{su} = T_{clock} - t_{PD} - t_{co}$



$200 = T_{clk} - 250 - 50$

$T_{clk} = 200 + 250 + 50 = 500\,ps$

$f_{clk} = 2\,GHz$

Exercise 5: Which of the above would increase design time? Which would increase the unit costs? Which would lower quality?

more time ⟷ change the design (e.g. pipelining).

more money → faster chip (cost)

lower quality → reduce clock rate