More Verilog

Exercise 1: Identify the module instantiation statements in the code above. For each one, what is the instantiated module's name? The instance name?

```
// matching by order
bits #(nbits) b0 (newest,a,clock);

// matching by name (order does not matter)
bits #(.nb(nbits)) b1 (.q(b),.clock,.d(a));

// wildcards for names that match
bits #(.nb(nbits)) b2 (.d(b),.q(oldest),.*);
```

module names

instance names

Exercise 2: How would you specify the bit marked ??? in the diagram above?

w[1][6]

Exercise 3: Write a Verilog lookup table to look up whether a value between 0 and 7 is a prime number or not. The result should be 1 if the value is a prime or else 0. *Hint: The primes are 2, 3, 5 and 7.*

0	0
1	0
2	1
3	1
4	0
5	1
6	0
7	1

```
logic isprime [0:7] = '{0,0,1,1,0,1,0,1};
```

examples:

isprime[3] == 1

isprime[0] == 0

Exercise 4: Is a signal named $\overline{\textbf{overload}}$ active-high or active-low? Is there an overload if this signal is high? What if the signal was named **overload**?

$\overline{\text{overload}}$ → active low ⇒ true when low

high ⇒ false

overload → active high ⇒ true when high

high → true

Exercise 5: Come up with active-high and an active-low names for a signal that is at 3 V when a door is open and 0 V when the door is closed.

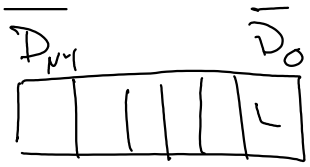
signal: 3 V = open

0 V = closed

active high: open

active low: $\overline{\text{closed}}$

Exercise 6: If $\overline{\text{D}}$ is ~~a data bus~~ word and $\overline{\text{D0}}$ is low, is the ~~value on the data bus an~~ word an even or odd number?



$\overline{D_0}$ = active low = true if low

= 1

∴ odd number