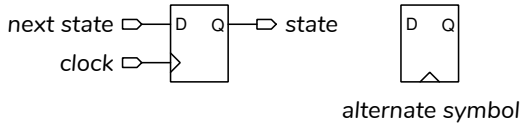
Flip-Flops and Registers

This lecture is an introduction to flip-flops and registers.
After this lecture you should be able to:

- *predict the relationship between the input and output waveforms of D flip-flops, registers, counters and shift registers*
- *draw block diagrams and write Verilog descriptions for these*

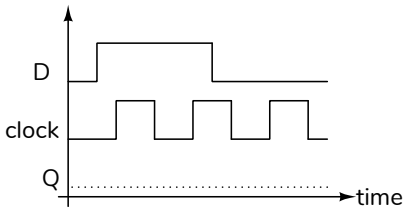
D Flip-Flop

The symbol for a D flip-flop is:



The rising edge of a clock input causes the flip-flop to store the value of the input and make it available on the output. Thus the D flip-flop has a next-state input (D), a state output (Q) and a clock input. The D flip-flop's state only changes on the rising edge of the clock.

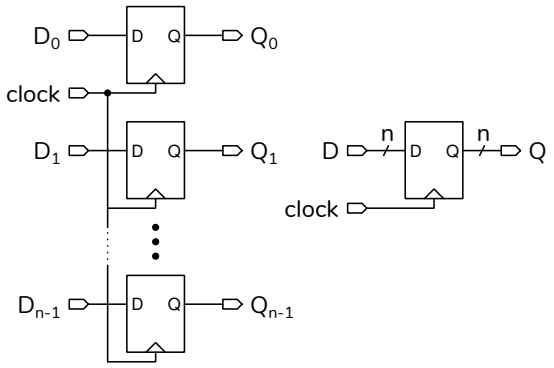
The D flip-flop "stores" one bit and is the memory element used in most sequential logic circuits.



Exercise 1: Fill in the waveform for the Q signal in the diagram above. Fill in with a shaded area if the value is unknown.

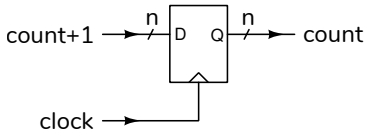
Common Sequential Logic Circuits

Register A register is multiple D flip-flops connected to the same clock so that all are loaded simultaneously. The notation on the right is for a register that is n bits wide.

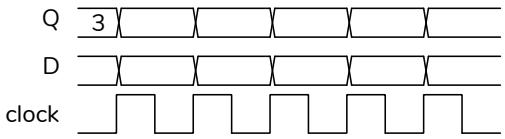


Exercise 2: What would be another name for a 1-bit register?

Counter A counter is a register whose value increases by 1 on each rising edge of the clock. It consists of a register whose input is the current value of the counter plus one:



On each clock edge the register loads a value that is one more than the previous value.

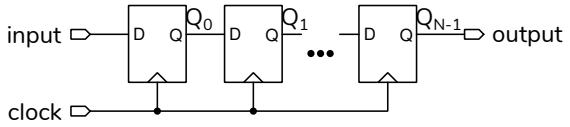


Exercise 3: Assuming a 3-bit counter, fill in the values of D and Q in the diagram above.

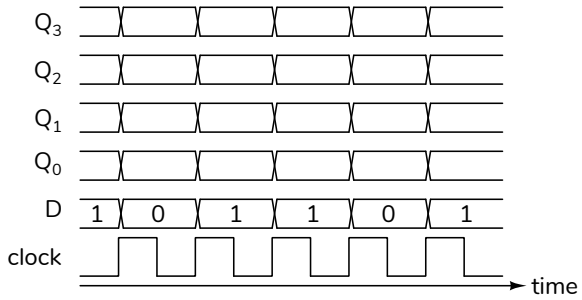
Exercise 4: Draw the block diagram for a counter that: (a) counts up by 3? (b) counts down by 1? (c) whose value doubles on each clock edge?

Exercise 5: Write the Verilog for each of the above.

Shift Register A shift register is several registers with the output of each register connected to the input of the next register:



On each rising edge of the clock the state of each register is transferred to the next one.



Exercise 6: Fill in the diagram above for a 4-bit shift register. Assume the initial value of each flip-flop is zero. Which is the oldest (first) value the D waveform? Which flip-flop holds the oldest value?

Exercise 7: Write the Verilog for a 4-bit shift register. The contents of the shift register should be stored in the array `q[3:0]` and the bits are shifted into `q[0]`.

A shift register makes previous inputs available in parallel. This is useful for detecting sequences and for transferring data serially.

Exercise 8: Draw a circuit that generates a signal named `detect` that is high when the sequence 1, 0, 1, 1, 0 is detected (on the input and stored in the shift register). Add the output of this circuit to the timing diagram above.

Exercise 9: Write the Verilog for this circuit.