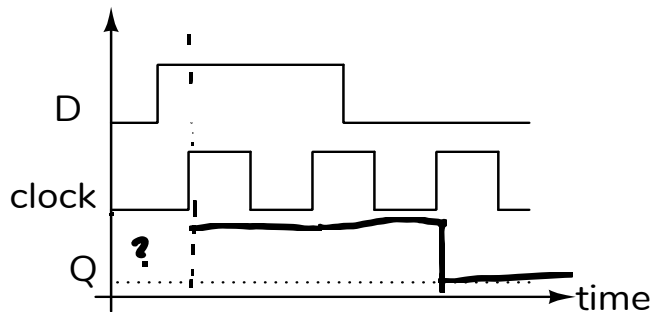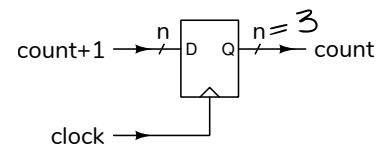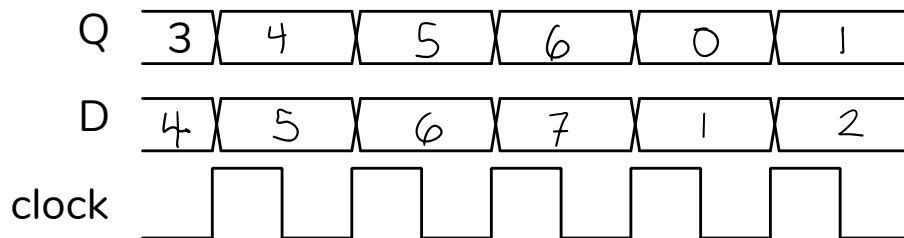# Flip-Flops and Registers

Exercise 1: Fill in the waveform for the Q signal in the diagram above. Fill in with a shaded area if the value is unknown.
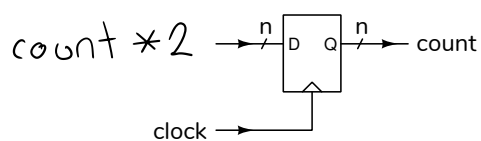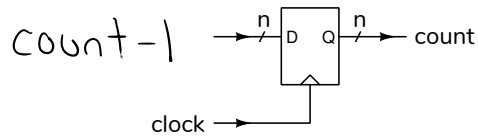

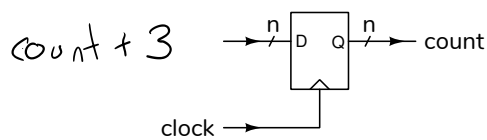**Exercise 2**: What would be another name for a 1-bit register?

    flip-flop

Exercise 3: Assuming a 3-bit counter, fill in the values of D and Q in the diagram above.

Q	3	4	5	6	0	1
D	4	5	6	7	1	2

clock

Exercise 4: Draw the block diagram for a counter that: (a) counts up by 3? (b) counts down by 1? (c) whose value doubles on each clock edge?
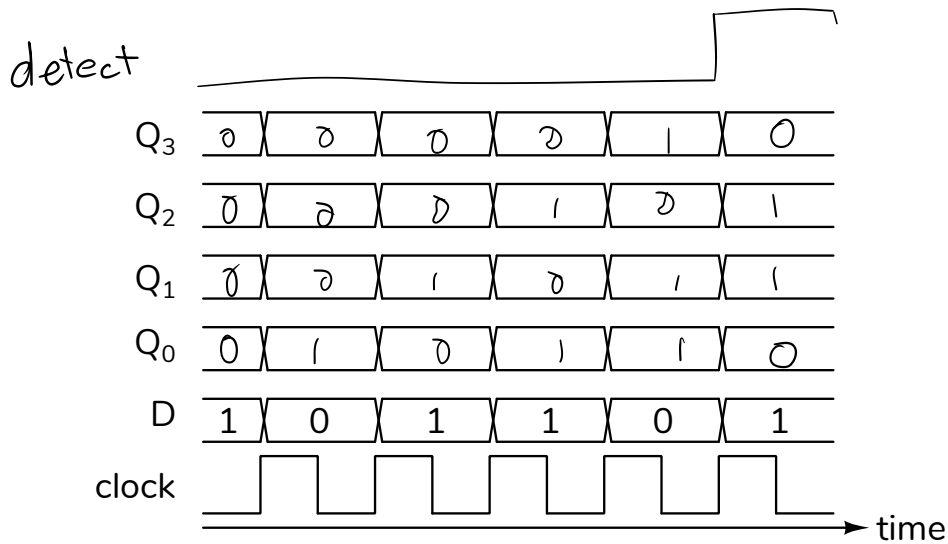
Exercise 5: Write the Verilog for each of the above.

```
always_ff @(posedge clock) count
   <= count + 1'b1 ;

always_ff @(posedge clock) count
   <= count - 1'b1 ;

always_ff @(posedge clock) count
   <= count * 2'b2 ;
```

Exercise 6: Fill in the diagram above for a 4-bit shift register. Assume the initial value of each flip-flop is zero. Which is the oldest (first) value the D waveform? Which flip-flop holds the oldest value?
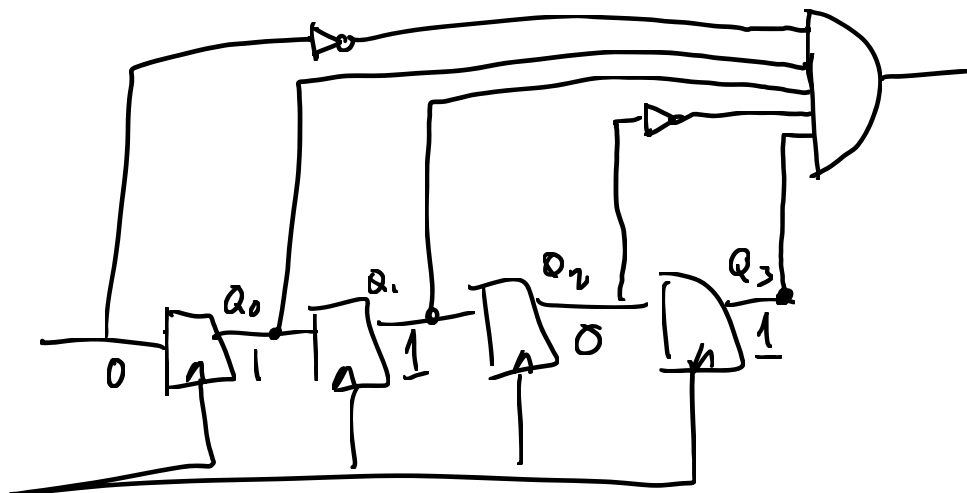
detect

Q_3	0	0	0	0	1	0
Q_2	0	0	0	1	0	1
Q_1	0	0	1	0	1	1
Q_0	0	1	0	1	1	0
D	1	0	1	1	0	1
clock						

→ time

```
Leftmost value in time is the oldest.
Rightmost flip-flop (Q3) holds the oldest value.
```

Exercise 7: Write the Verilog for a 4-bit shift register. The contents of the shift register should be stored in the array q[3:0] and the bits are shifted into q[0].

```
always_ff @(posedge clock) q <= {q[2:0],d} ;
```

Exercise 8: Draw a circuit that generates a signal named detect
that is high when the sequence 1, 0, 1, 1, 0 is detected (on the input
and stored in the shift register). Add the output of this circuit to the
timing diagram above.

Exercise 9: Write the Verilog for this circuit.

Q_3 Q_0
1   0   1   1   0

```
assign detect = {q[3:0],d} == 5'b10110 ;
```