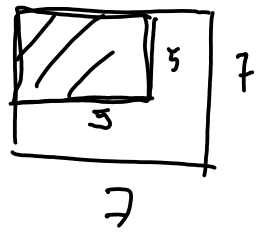
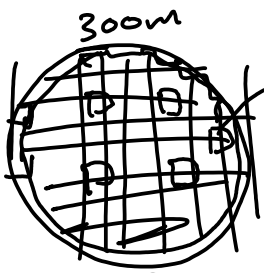
Programmable Logic Applications and Architectures

Exercise 1: What improvement in number of transistors per unit area would be achieved by reducing the transistor dimensions from 7 nm to 5 nm? Approximately how many 5x5 mm die fit on a 300 mm wafer? How many 200x200 nm gates fit on the die?



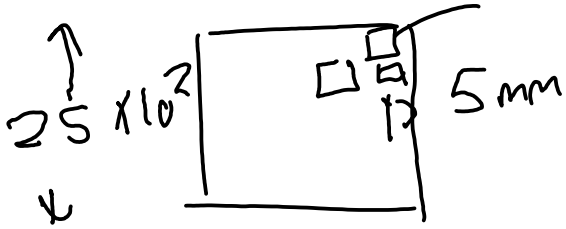
$\frac{7 \times 7}{5 \times 5} = \frac{49}{25}$.



$5\times5\ N = \frac{\pi r^2}{5\times5} = \frac{2\pi (150)^2}{25}$

$= 2500$

5mm



$\frac{5 \times 10^{-3}}{0.2 \times 10^{-6}}$

$= 25 \times 10^3$ ← on each side

$@ 25 \times 10^6$ gates

25×10^3

Exercise 2: Would you use hardware or software to implement: A calculator? A controller for kitchen appliance? An Ethernet interface? To do Bitcoin "mining"?

	operations	time	clock cycles	$\frac{OPS}{clock}$
calculator	100 ?	≈ 0.1s	10^6 @ 10MHz	<<1
appliance	100 ?	≈ 1s	10^7 10MHz	<<1
Ethernet @ 1Gb/s	10 ?	1×10^{-9} s	10^{-1} @100MHz	>>1
Bitcoin	?	no limit	?	?

Exercise 3: Would you use a PLD or ASIC for: A project that had to be completed within a month? That would be expected to sell 100 million units? Whose complete requirements aren't known? A state-of-the-art general-purpose CPU?

- TTM $\approx$ 1 month $\rightarrow$ PLD
- 100×10^6 units $\rightarrow$ ASIC
- need to upgrade $\rightarrow$ PLD
- high performance $\rightarrow$ ASIC