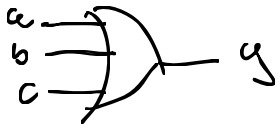
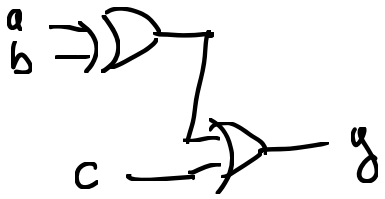
Introduction to Digital Design with Verilog HDL

Exercise 1: What changes would result in a 3-input OR gate?

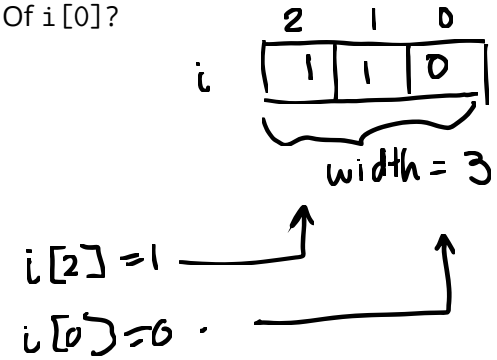
```
module ex1 ( input logic a, b, c,
             output logic y );

assign y = a | b | c;

endmodule
```



Exercise 2: What schematic would you expect if the statement was `assign y = ( a ^ b ) | c ;?`



Exercise 3: If the signal `i` is declared as `logic [2:0] i;`, what is the 'width' of `i`? If `i` has the value 6 (decimal), what is the value of `i[2]`? Of `i[0]`?



Exercise 4: What are the ~~sizes~~ length and values, in decimal, of the following: `4'b1001`, `5'd3`, `6'h0_a`, `3`?

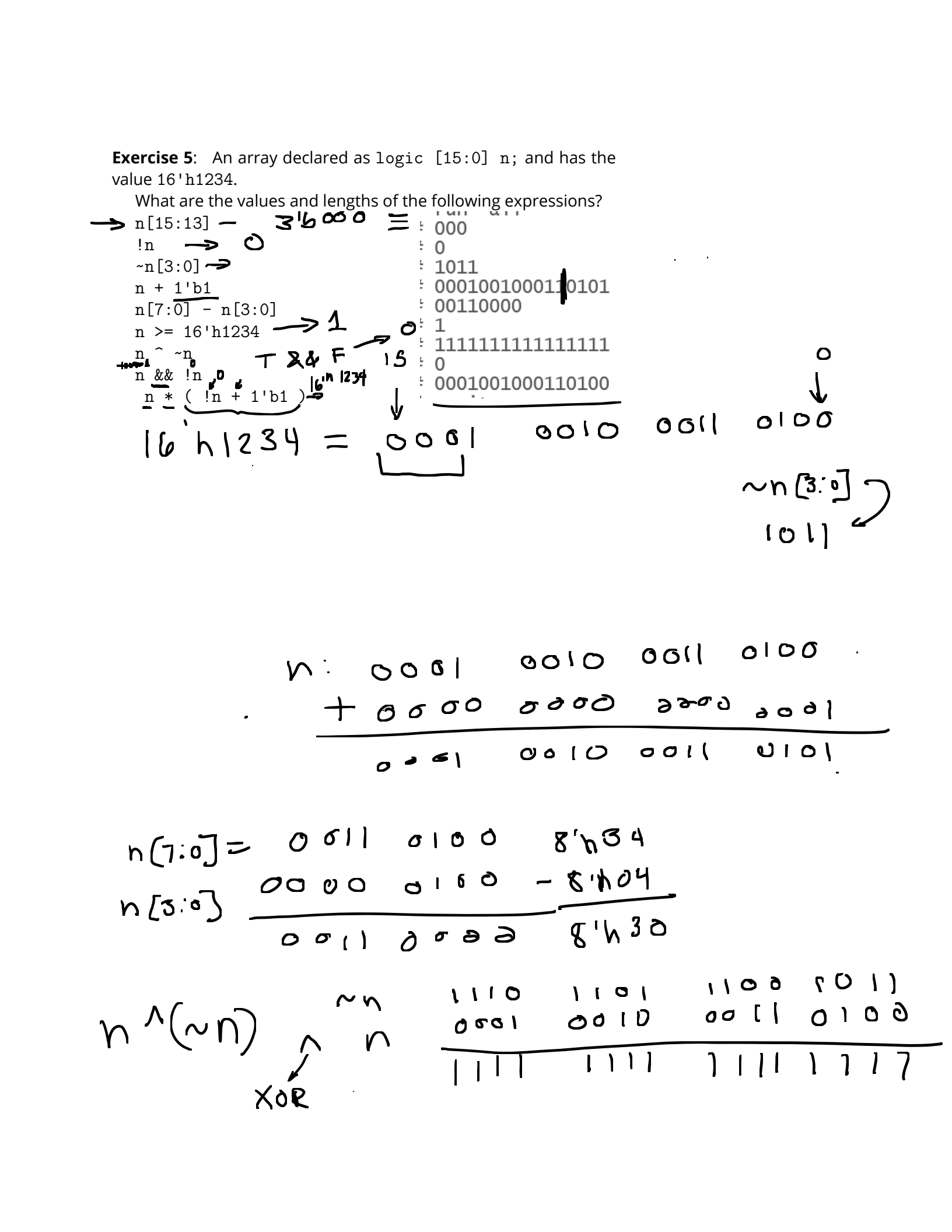
	length	value
4'b1001	4	9
5'd3	5	3
6'h0_a	6	10
3	32	3

Exercise 5: An array declared as `logic [15:0] n;` and has the value `16'h1234`.

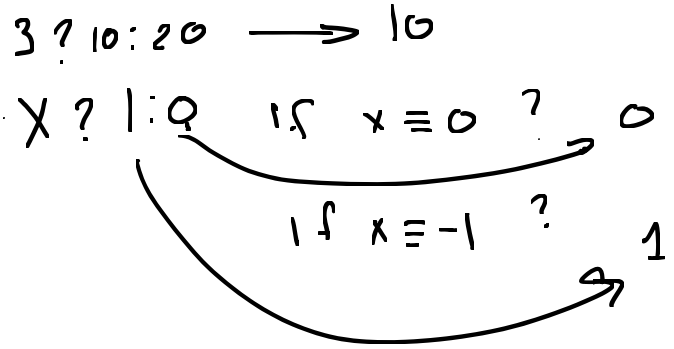
What are the values and lengths of the following expressions?

```
n[15:13]
!n
~n[3:0]
n + 1'b1
n[7:0] - n[3:0]
n >= 16'h1234
n ^ ~n
n && !n
n * ( !n + 1'b1 )
```

```
000
0
1011
0001001000110101
00110000
1
1111111111111111
0
0001001000110100
```

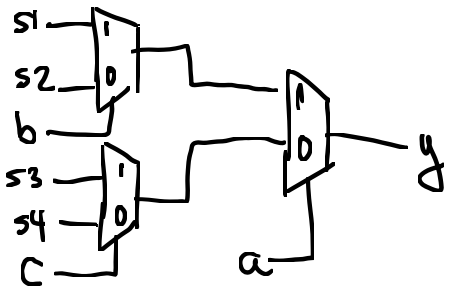


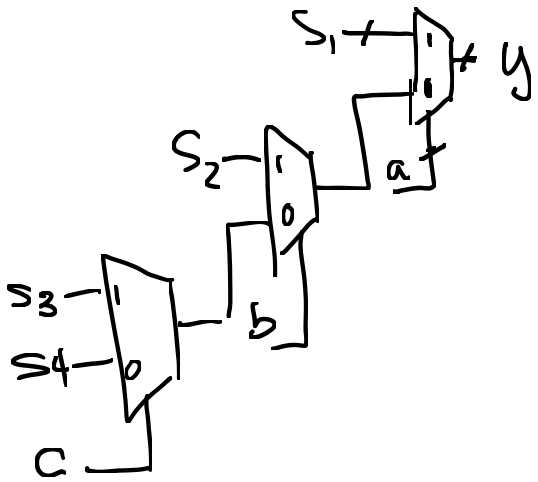
Exercise 6: What is the value of the expression `3 ? 10 : 20`? Of the expression `x ? 1 : 0` if `x` has the value 0? If `x` has the value -1?



Exercise 7: Draw the schematics corresponding to:

```
y = a ? ( b ? s1 : s2 ) : ( c ? s3 : s4 );
y = a ? s1 : b ? s2 : c ? s3 : s4;
```

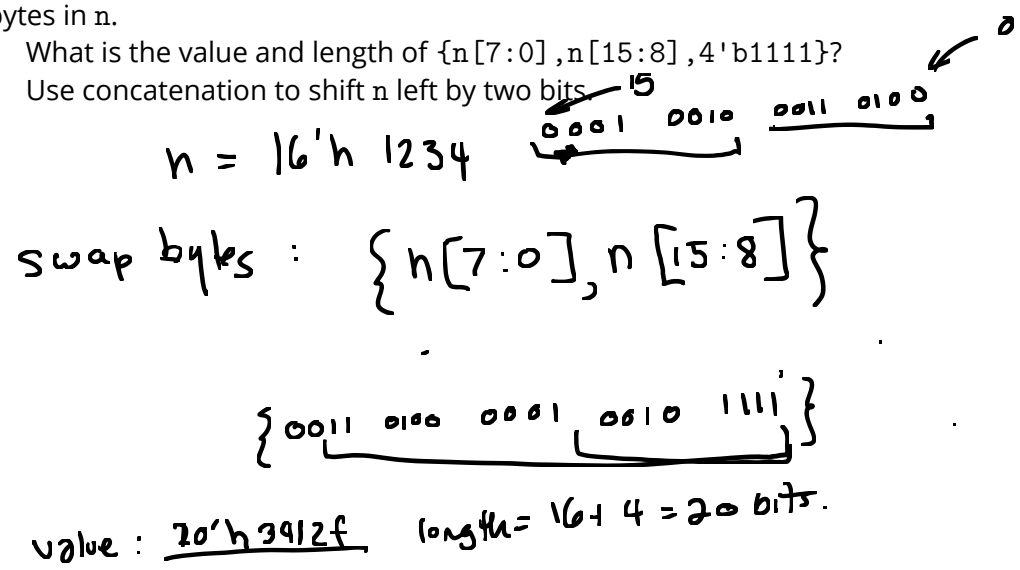




Exercise 8: Use slicing and concatenation to swap the order of the bytes in `n`.

What is the value and length of `{n[7:0],n[15:8],4'b1111}`?

Use concatenation to shift `n` left by two bits.



Shift left by 2 bits

{n, 2'b00} → 18 bits

{n[13:0], 2'b00} → 16 bits

Exercise 9: What would you change to make an 8-bit register? A 4-bit counter? A 3-bit shift register? Follow the course coding conventions.