# Logic Level Conversion

*Revised: March 21.*

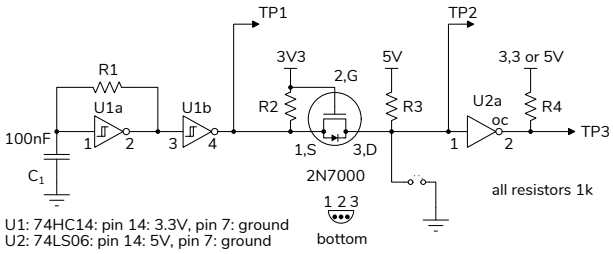
## Introduction

Voltages used in logic circuits are a compromise between power consumption and noise immunity.

ICs made with bipolar transistors typically use 5 V logic levels. ICs made with CMOS transistors often use 3.3 V IO logic levels.

When both types of devices are used in the same circuit it's necessary to convert between different logic levels. In this lab you will build and test circuits that do this.

The lectures describe simple techniques, such a voltage dividers, diode clamps and MOSFET switches to convert between logic levels. In this lab you will build and test the two logic level conversion circuits shown in the schematic below:




U1a and U1b form an RC oscillator using 74HC14 CMOS Schmitt trigger input inverters as in a previous lab. The supply voltage, and thus the logic levels are 3.3 V.

U2 is a hex 74LS06 TTL open-collector inverter. The supply voltage, and thus the logic levels, are 5 V.

The circuit between U1 and U2 uses a 2N7000 N-channel MOSFET to convert the 3.3V output of U1 to a 5 V input for U2:

- When the source is low, the gate-source voltage ($V_{GS}$) is 3.3 V, the transistor conducts and the drain terminal is pulled low.
- When source is high, $V_{GS}$ is 0 V, the transistor is off and the drain terminal is pulled up to 5 V.

The interesting feature of this circuit it that pulling the drain terminal low pulls the source low through the "body diode"[1]. This allows bidirectional logic level conversion between two open-collector outputs. For example, a sensor with a 5 V I2C interface and a microcontroller with 3.3 V IO.

U2 is a 74LS06 hex open-collector inverter. The outputs can be pulled up to any voltage up to 30 V. The output can sink up to 40 mA, enough to drive small loads directly or as a driver for higher-power semiconductors. Since $V_{IH}$ is 2 V it can be driven from a 3.3 V CMOS logic output. This IC can thus convert 3.3 V or 5 V logic levels to any other logic level.

## Components

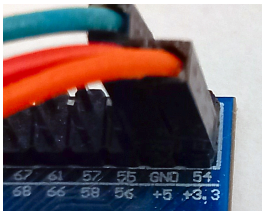
You will need the following from your ELEX 2117 parts kit:

- 74HC14 hex Schmitt trigger input inverter
- 74LS06 hex open-collector inverter
- 2N7000 n-channel MOSFET
- 4×1 kΩ resistors (from your ELEX 1117 parts kit)
- 100 nF capacitor
- your breadboard, some hookup wire and M-F jumpers
- your AD2 (you may use the lab 'scopes instead if you have a USB flash drive)

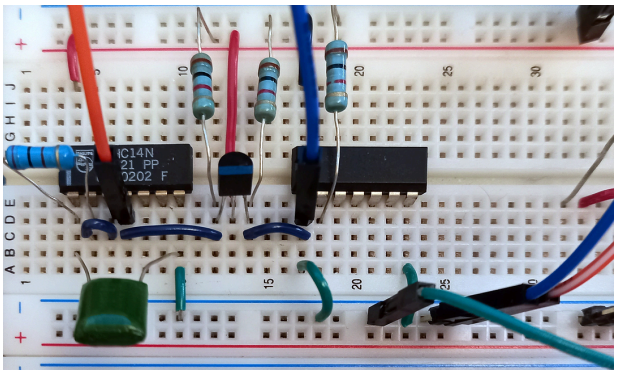
## Procedure

Build the circuit shown above on your breadboard. You can use the 5 V and 3.3 V supplies from the CPLD board (the ground, 3.3 V and 5 V pins are on the pin headers at the upper right of the board):

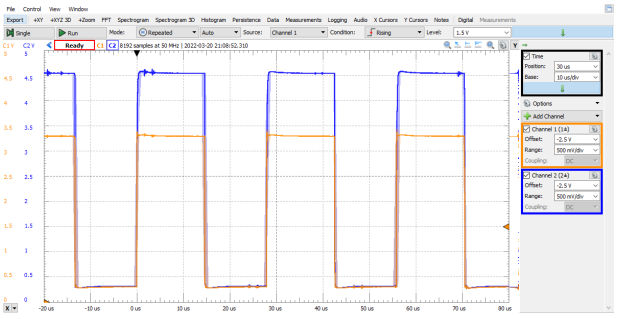
[1] MOSFETs are actually 4-terminal devices. For an n-channel transistor the control voltage is applied between the gate and the P substrate. In most packages the P substrate is connected to the source. This results in a PN "body" diode from source to drain as shown above and in some MOSFET schematic symbols.




The diagram below shows an example of how it could be built. Note the two supply rails (one for 5 V and one for 3.3 V).



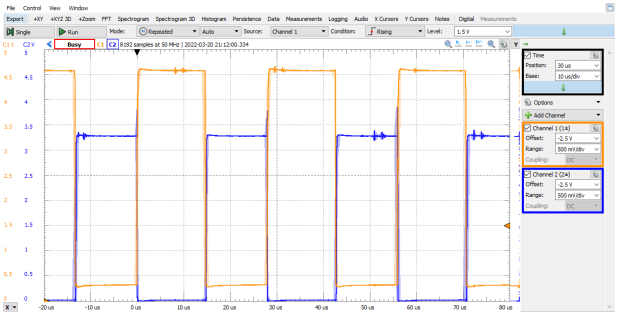
Connect the AD2 (or lab) 'scope channel 1 input to test point 1 (TP1) and channel 2 to TP2. You should see a 3.3 V clock signal on channel 1 and a 5 V clock signal on channel 2 as shown below:



Ground the drain (TP2, U2 pin 1, channel 2)[2] and observe the effect on the source voltage (TP1, U1 pin 4, channel 1).

Now switch channel 1 to TP2 and channel 2 to TP3. If the pull-up is connected to 3.3 V you should see the output inverted but at 3.3V:

[2]Do this briefly; U2 does not have open-collector outputs but should tolerate its output being short-circuited briefly.



Switch the pull-up resistor to 5 V and observe the effect on the output.

## Report

Show your working circuit to the instructor to get a mark for completing the lab. If you complete the lab at home, include a photo of your circuit in your report.

Your report should include the following:

- The waveforms at TP1 and TP2 showing the voltage levels over one or more periods of the waveform.
- Describe what happens when you ground TP2.
- The waveforms at TP2 and TP3 showing the voltage levels over one more more periods of the waveform.
- Describe what happens when you switch the pull-up from 3.3 V to 5 V.

Do *not* use your phone camera to record the lab 'scope screen! Instead, plug your USB flash drive into the USB Flash Drive socket on the 'scope and configure the 'scope to save screen images when you push the PRINT button by using the menu options: SAVE/RECALL / Save All / PRINT Button : Saves Image to File: