Matrix Keypad Decoder

Introduction

In this lab you will design a circuit to scan the matrix keypad and display the digit that is being pressed (0 through 9) on the rightmost digit of the LED display. Pressing the * and # keys will display the last two digits of your BCIT ID.

You will use the same components as in the previous lab, connected the same way.

Matrix Keypad

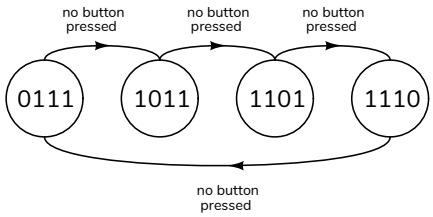
Review the description of the matrix keypad in a previous lab.

Design

In order to determine which button, if any, is being pressed your design must set one row output low and check to see if any of the column inputs is low. If any are low, then the button at the intersection of the low row and the low column is being pressed. If not, then no button along that row is being pressed and your circuit should proceed to the test the next row.

Your circuit should continuously test each of the rows in order from top to bottom and stop scanning when it detects that a button is being pressed. It should resume scanning when no button is being pressed.

The state transition diagram for the row output sequence generator is:

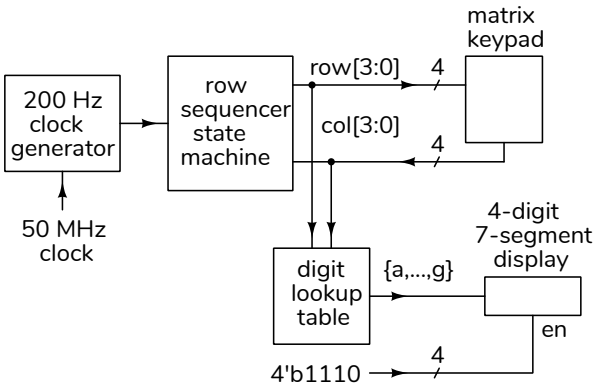


where the state is the binary value of the `row[3:0]` output.

The scanning rate should be 200 Hz, determined by a clock generated as in the previous lab.

The digits displayed for * and # should be the second-last and last digits of your BCIT ID. For example, if your ID were A00123456 then pressing * should display 5 and pressing # should display 6.

A possible block diagram for your design is:



Component Connections

The CPLD board, keypad and LED display should be connected as in the previous lab.

Procedure

Follow the general procedure in the Software Installation and Use document on the course website to create a project, compile it and configure the CPLD.

You can import the pin assignments as described in the previous lab. Remember to enable the internal pull-up resistors on the column inputs.

You can instantiate a 200 Hz clock generator as described in the previous lab.

Connect the keypad and LED to the CPLD board. Compile your design and program the CPLD. Test your design and fix any errors.

Hints

Your design will consist of:

1. A state machine that sequences through four states in order from top to bottom as shown above.

2. A combinational logic circuit that sets the LED segments corresponding to the row and column that are low. For example if the second column from the left (2) is low when the bottom row (0) is set low then `0.` should be displayed on the rightmost digit of the LED display.

3. You can concatenate the row and column values to create an 8-bit value. For example, you could use the expression `{row,col} == 8'b1110_1011`.

By default the CPLD registers will power up with a value of zero. Make sure your state machine will work properly if it starts at the all-zero state (e.g. design it so that it recovers from any invalid state).

You can use the **`lab3.pof`** file on the course website to test your hardware and view the lab3demo video for an example of the required behaviour.

Submissions

Lab Report

Submit the following to the appropriate Assignment folder on the course website:

1. A PDF document containing:

   - A listing of your Verilog code.
   - A screen capture of your compilation report. For example:

Flow Status	Successful - Sat Jan 29 21:28:17 2022
Quartus Prime Version	21.1.0 Build 842 10/21/2021 SJ Lite Edition
Revision Name	lab3
Top-level Entity Name	lab3
Family	MAX II
Device	EPM240T100C5
Timing Models	Final
Total logic elements	79 / 240 (33 %)
Total pins	20 / 80 (25 %)
Total virtual pins	0
UFM blocks	0 / 1 (0 %)

2. If you were not able to demonstrate your solution to the lab instructor during your scheduled lab period, submit a video showing the keypad and the LED display as you push the keys 0 through 9, the `*` and `#` keys and the `A` through `D` keys.

Follow the *Report and Video Guidelines* and *Coding Guidelines* documents on the course website.