ELEX 2117 : Digital Techniques 2
2022 Winter Term

FINAL EXAM
14:30 – 17:30
Thursday, April 14, 2022
NE01-331 or NE01-209

This exam has eleven (11) questions on three (3) pages. The marks for each question are as indicated. There are a total of thirty-six (36) marks. Answer all questions. Write your answers and all rough work in this paper and nowhere else. Show your work. Draw a box around your final answer. Numerical answers must include units. Books and notes are allowed. No electronic devices other than calculators are allowed. **Show your work.**

This exam paper is for:

Sample Exam 1 A00123456

Each exam is equally difficult.

Answer your own exam.

Do not start until you are told to do so.

Name: _____

BCIT ID: _____

Signature: _____

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Question 1 — 4 marks

Write a Verilog module named **swap** with two 8-bit inputs named **b0** and **b1**, a one-bit input named **little**, and a 16-bit output named **w**. The output **w** is set as follows:

- when **little** is high, **w** is set to a 16-bit value with **b0** as the most significant byte and **b1** as the least significant byte.
- when **little** is low, **w** is set to a 16-bit value with **b1** as the most significant byte and **b0** as the least significant byte.

Follow the mandatory course coding guidelines except that you need not include comments.

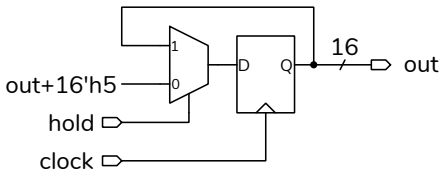
Question 2 — 4 marks

A state machine has a one-bit **step** input, a one-bit **reset** input, a **clock** input, and an 8-bit **value** output. The value of **value** changes only on the rising edge of **clock**. If **reset** is asserted, **value** is set to **8'h00**. Otherwise if **step** is asserted **value** is incremented by 5. Otherwise **value** is held at the same value. You do not need to consider a possible overflow of **value**.

Write a Verilog module named **stepper** that implements this state machine. Follow the mandatory course coding guidelines except that you need not include comments.

Question 3 — 4 marks

Write a Verilog module corresponding to the diagram shown at right. **hold** and **clock** are one-bit inputs and **out** is a 16-bit output. **out** in the expression is the same signal as the output. Follow the mandatory course coding guidelines except that you need not include comments.



4in

Question 4 — 5 marks

Given the following Verilog declarations:

```
logic [11:0] x = 16'd45 ;
logic  [3:0] y = 4'b101 ;
```

fill in in the table below with the value of the each expression as a hexadecimal (base 16) number (Verilog format not necessary) and the length (number of bits) as a decimal (base 10) number:

expression	value (in hexadecimal)	length (in bits, decimal)
`{x,y}`		
`x[7:4]`		
`x & y`		
`x - y`		
`x[0] ? y : ~y`		

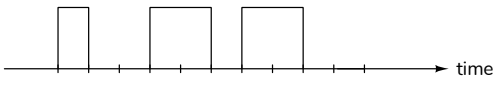
Question 5 — 3 marks

Fill in the blank boxes in the table below so that all values in each row are consistent (agree with each other). The first row is an example.

signal name	truth value (T/F)	logic level (H/L)	Verilog value as output (0/1)	Verilog value in expression (0/1)
$\overline{\texttt{hot}}$	T	L	0	1
running	F			
odd*		L		
$\overline{\texttt{failed}}$	F			

Question 6 — 4 marks

The waveform at right is measured on an asynchronous serial interface. Tic marks on the time axis mark bit periods. The bit order and levels follow the standard for asynchronous serial interfaces. An 8-bit value was transferred. The diagram shows the complete transmission of one byte, including any additional bits required for synchronization.



What value was transmitted over the interface? Give your answer as a Verilog constant with the correct width and a hexadecimal base. Show how you obtained your answer.

Question 7 — 3 marks

A sequential logic circuit uses registers with a minimum setup time requirement of 2 ns and a maximum clock-to-output delay of 3 ns. It needs to run at a clock rate of 40 MHz. What is the maximum allowable propagation delay through any combinational logic path in the circuit? Show your work and include units in your answer.

Question 8 — 4 marks

You need to design a 128 kByte memory for a 16-bit CPU using 32 k × 4 memory ICs.

(a) How many address bits does each memory IC have? 0.75in

(b) How many IC's will be needed for each bank? 0.75in

(c) How many banks will be required? 0.75in

(d) If an address decoder places the first byte of this memory at address **`0x10 0000`**, what is the last address in this memory? 0.75in

Question 9 — 2 marks

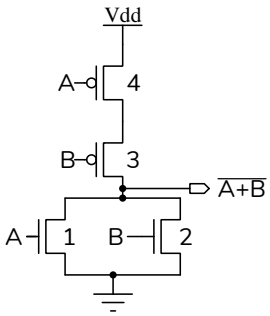
You are choosing the logic levels for a new design and need to maintain a noise margin of 1 V for both high and low logic levels. $V_{IL(max)}$ is 2 V and $V_{IH\ (min)}$ is 3 V. What are $V_{OL(max)}$ and $V_{OH(min)}$?

Question 10 — 2 marks

A CMOS digital logic circuit consumes 100 mW at a supply voltage of 5 V and a clock frequency of 5 MHz. The clock frequency is reduced to 1 MHz and the supply voltage to 3 V. What is the new power consumption?

Question 11 — 1 marks

The schematic at right shows a CMOS NOR gate with the four transistors numbered from 1 to 4. Both A inputs are at the same logic level. Both B inputs are at the same logic level. Which transistors are on (conducting) when the output is high?



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This exam paper is for:

Sample Exam 2 A01234567

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Name: _____

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Question 1 — 4 marks

Write a Verilog module named **swap** with two 8-bit inputs named **b0** and **b1**, a one-bit input named **big**, and a 16-bit output named **w**. The output **w** is set as follows:

- when **big** is high, **w** is set to a 16-bit value with **b1** as the most significant byte and **b0** as the least significant byte.
- when **big** is low, **w** is set to a 16-bit value with **b0** as the most significant byte and **b1** as the least significant byte.

Follow the mandatory course coding guidelines except that you need not include comments.

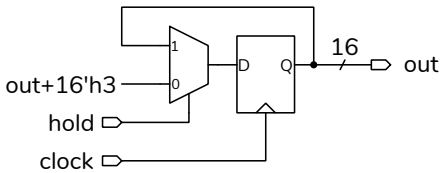
Question 2 — 4 marks

A state machine has a one-bit **step** input, a one-bit **reset** input, a **clock** input, and an 8-bit **value** output. The value of **value** changes only on the rising edge of **clock**. If **reset** is asserted, **value** is set to **8'hff**. Otherwise if **step** is asserted **value** is decremented by 3. Otherwise **value** is held at the same value. You do not need to consider a possible underflow of **value**.

Write a Verilog module named **stepper** that implements this state machine. Follow the mandatory course coding guidelines except that you need not include comments.

Question 3 — 4 marks

Write a Verilog module corresponding to the diagram shown at right. **hold** and **clock** are one-bit inputs and **out** is a 16-bit output. **out** in the expression is the same signal as the output. Follow the mandatory course coding guidelines except that you need not include comments.



4in

Question 4 — 5 marks

Given the following Verilog declarations:

```
logic [15:0] x = 16'd90 ;
logic  [3:0] y = 4'b111 ;
```

fill in in the table below with the value of the each expression as a hexadecimal (base 16) number (Verilog format not necessary) and the length (number of bits) as a decimal (base 10) number:

expression	value (in hexadecimal)	length (in bits, decimal)
`{x,y}`		
`x[7:4]`		
`x & y`		
`x - y`		
`x[0] ? y : ~y`		

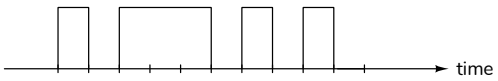
Question 5 — 3 marks

Fill in the blank boxes in the table below so that all values in each row are consistent (agree with each other). The first row is an example.

signal name	truth value (T/F)	logic level (H/L)	Verilog value as output (0/1)	Verilog value in expression (0/1)
$\overline{\texttt{hot}}$	T	L	0	1
running	T			
odd*		H		
$\overline{\texttt{failed}}$	T			

Question 6 — 4 marks

The waveform at right is measured on an asynchronous serial interface. Tic marks on the time axis mark bit periods. The bit order and levels follow the standard for asynchronous serial interfaces. An 8-bit value was transferred. The diagram shows the complete transmission of one byte, including any additional bits required for synchronization.



What value was transmitted over the interface? Give your answer as a Verilog constant with the correct width and a hexadecimal base. Show how you obtained your answer.

Question 7 — 3 marks

A sequential logic circuit uses registers with a minimum setup time requirement of 4 ns and a maximum clock-to-output delay of 4 ns. It needs to run at a clock rate of 50 MHz. What is the maximum allowable propagation delay through any combinational logic path in the circuit? Show your work and include units in your answer.

Question 8 — 4 marks

You need to design a 256 kByte memory for a 16-bit CPU using 64 k × 4 memory ICs.

(a) How many address bits does each memory IC have? 0.75in

(b) How many IC's will be needed for each bank? 0.75in

(c) How many banks will be required? 0.75in

(d) If an address decoder places the first byte of this memory at address **`0x10 0000`**, what is the last address in this memory? 0.75in

Question 9 — 2 marks

You are choosing the logic levels for a new design and need to maintain a noise margin of 1.5 V for both high and low logic levels. $V_{IL(max)}$ is 2 V and $V_{IH\ (min)}$ is 3 V. What are $V_{OL(max)}$ and $V_{OH(min)}$?

Question 10 — 2 marks

A CMOS digital logic circuit consumes 100 mW at a supply voltage of 5 V and a clock frequency of 10 MHz. The clock frequency is reduced to 1 MHz and the supply voltage to 3 V. What is the new power consumption?

Question 11 — 1 marks

The schematic at right shows a CMOS NOR gate with the four transistors numbered from 1 to 4. Both A inputs are at the same logic level. Both B inputs are at the same logic level. Which transistors are on (conducting) when the output is high?