Timing Analysis

Exercise 1: Which of the specifications in the formula above decrease the available setup time as they increase? Which increase it?

$$t_{SU} = T_{clock} - t_{CO} - t_{PD}$$

increases t_{su}.

decreases t_{su} (available)

Exercise 2: For a particular circuit f_{clock} is 50 MHz, t_{CO} is 2 ns (maximum), the worst-case (maximum) t_{PD} in a circuit is 15 ns and the minimum setup time requirement is 5 ns. What is the setup time

clock frequency at which it will?

$f_{clock} = 50$ MHz $\Rightarrow T_{clock} = \frac{1}{50 \times 10^{6}} = .02 \times 10^{-6} = 20$ ns

$t_{su\,(available)} = T_{clock} - t_{co} - t_{PD}$

$= 20 - 2 - 15 = 3$ ns.

slack $= t_{su\,(avail)} - t_{su\,(min)}$

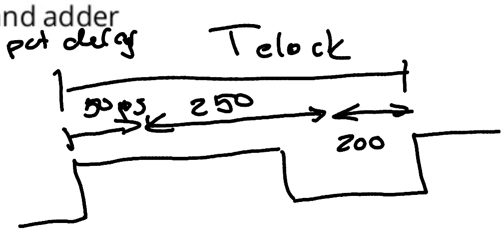
$= 3 - 5 = -2$

need to add 2ns to clock period

min clock period will be $20 + 2 = 22$ ns.

max clock freq. $= \frac{1}{22 \text{ ns}} \approx 45$ MHz

Exercise 3: What is the maximum clock frequency for a counter using flip-flops with 200 ps setup times, 50 ps ~~hold~~ times and adder logic that has a 250 ps propagation delay? clock - output delay



$t_{SU} = 200ps$

$t_{CO} = 50\ ps$

$t_{PD} = 250ps$

minimum clock period = $50 + 250 + 200 = 500ps$.

max clock freq. $= \frac{1}{0.5 \times 10^{-9}} = 2\ GHz$.

Exercise 4: Which of the above would increase design time? Which would increase the unit costs? Which would lower quality?

- Change the design to speed up critical timing paths. This might mean having more logic in parallel or "pipelining" – dividing up the computation across multiple clock cycles.
- Use a faster device – one with lower t_{PD} and/or t_{SU}.
- Relax the design constraints by reducing the clock rate.
- Reduce the interconnect delays by asking the EDA software to spend more time (effort) in the place-and-route (PAR) process and/or using a larger PLD.

increase design time	increase unit cost	lowers product quality
Y	N	N
N	Y	N
N	N	Y
N	N	N

- . speed significantly).