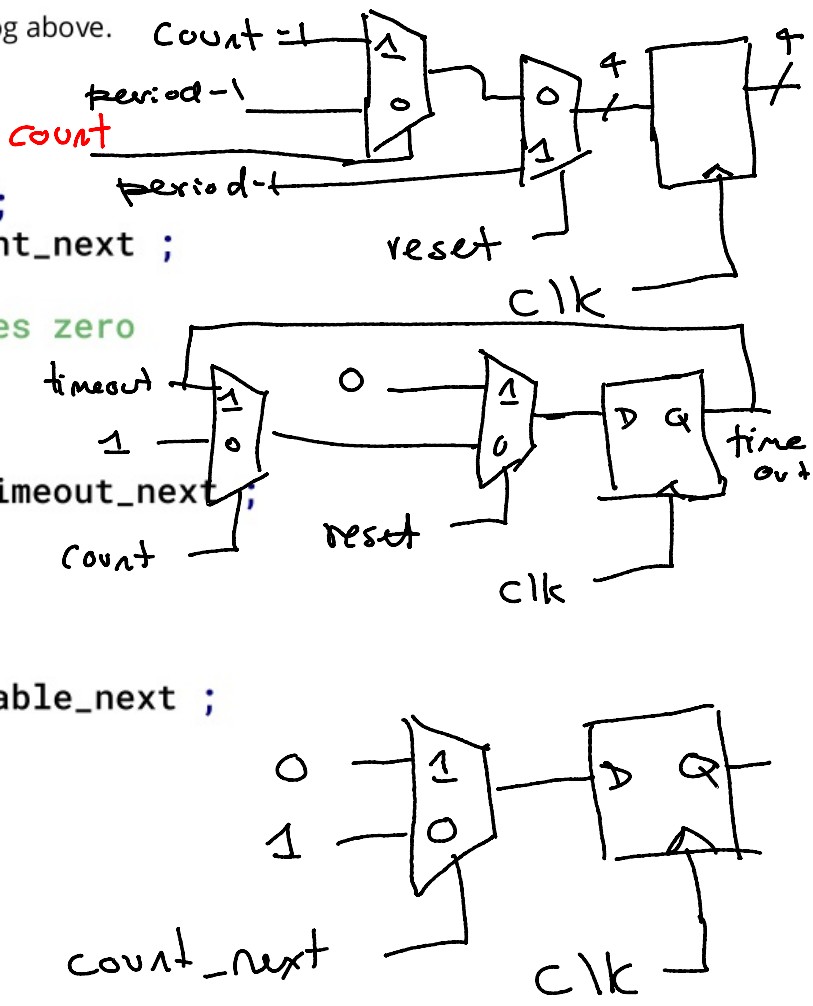
Common Circuits

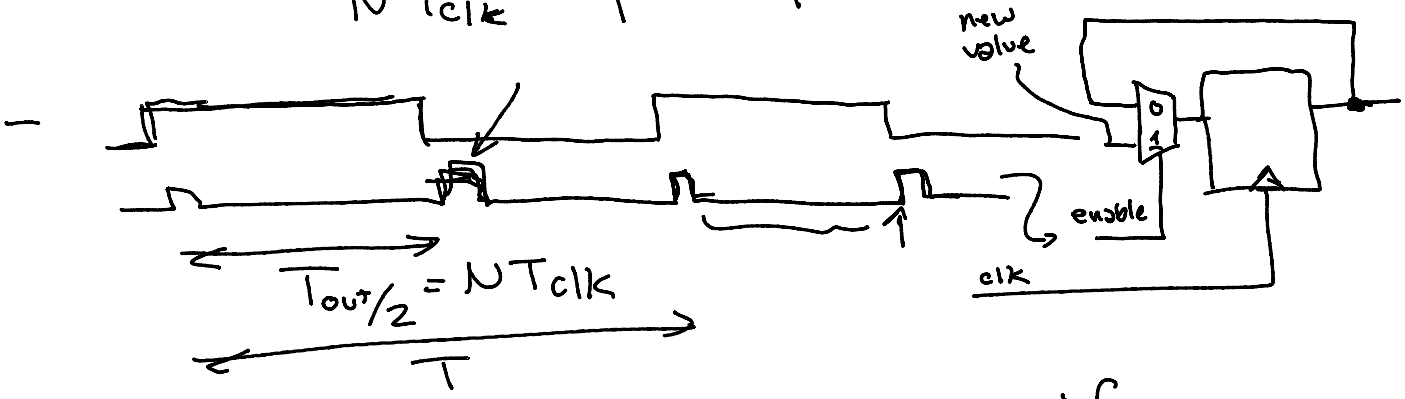
Exercise 1: Draw the block diagram for the Verilog above.

```
// resetable clock divider
assign count_next
  = reset ? period-1 :
    count ? count - 1'b1 : period-1 ;
always_ff @(posedge clk) count = count_next ;

// latch a '1 first time count reaches zero
assign timeout_next
  = reset ? '0 :
  count ? timeout : '1 ;
always_ff @(posedge clk) timeout = timeout_next ;

// periodic signal
assign enable_next
  = count_next ? '0 : '1 ;
always_ff @(posedge clk) enable = enable_next ;
```

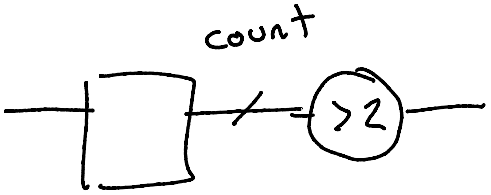


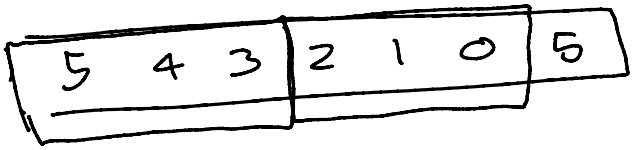
Exercise 2: Is the enable output a square wave? How could you create a square wave? What would be the period?

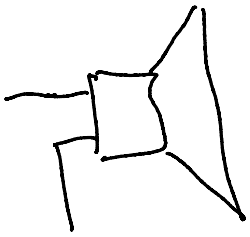
- enable o/p is pulses with period $N T_{clk}$ but pulse duration is T_{clk}

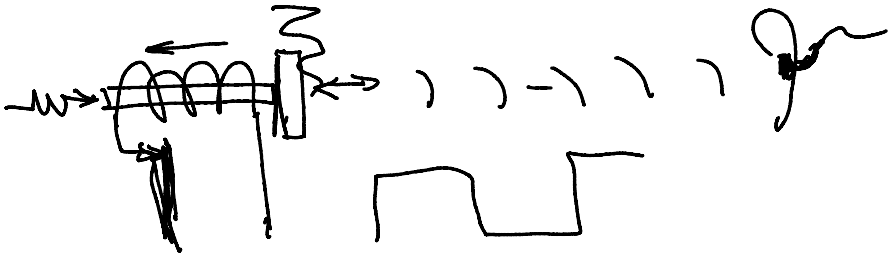


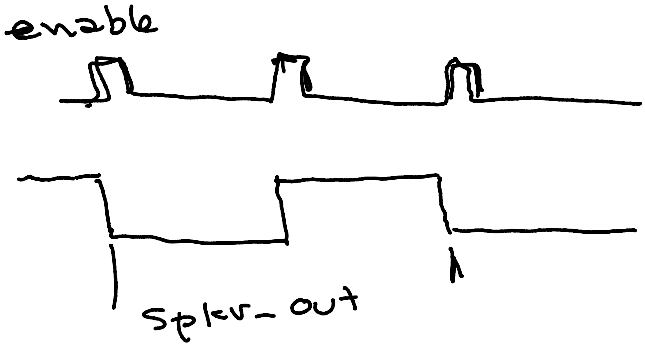
- period would be $2NT_{clock}$ if toggle o/p on each enable

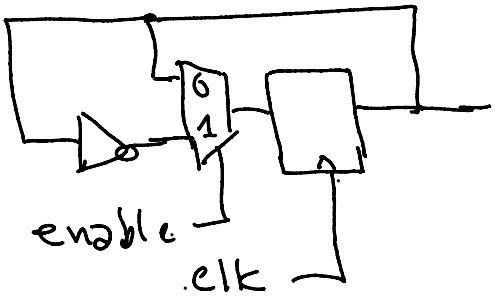




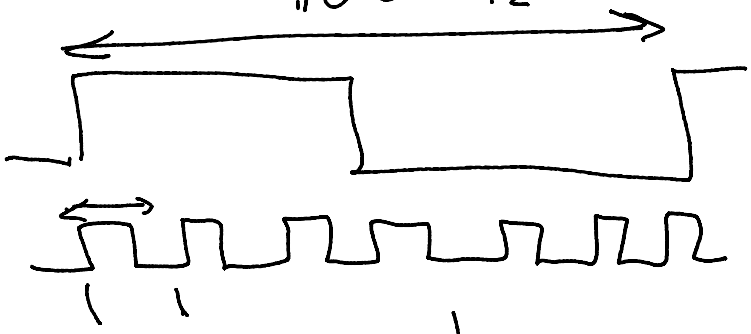








$$\frac{1}{100\ Hz} = 10\ ms.$$



$$\frac{10\ ms}{20ns} =$$

$$20ns = \frac{1}{50MHz}$$

$$\frac{10 \times 10^{-3}}{20 \times 10^{-9}}$$

$$= 0.5 \times 10^{6}$$

$$= 500{,}000$$

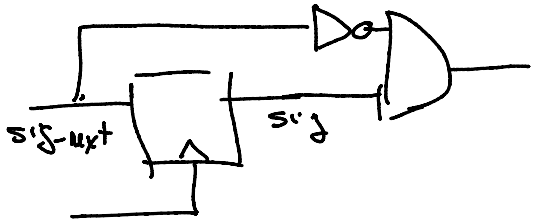
Exercise 3: How would the output differ if `enable_next` was based on `count` rather than `count_next`?

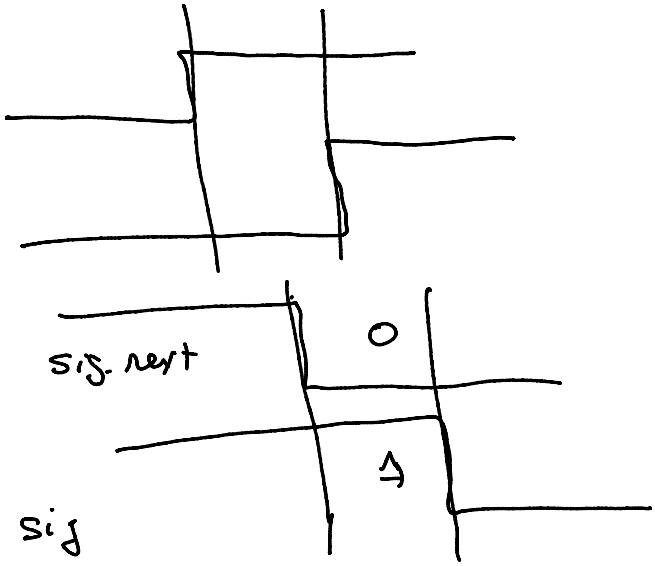
it would be delayed by 1 clock period

Exercise 4: What is the duration of the `sig_rising` output?

1 clock period.

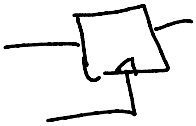
Exercise 5: How would you detect a falling edge?





Exercise 6: Draw the schematic of a synchronizer.

a FF



Exercise 7: What is the bounce duration in the waveform above? What value of `N` would achieve a delay of ten times this with a 50 MHz clock?

≈ 1 ms.

10 ms with 20ns clock period.

$$\frac{10\text{ ms}}{20\text{ns}} = \frac{10\times10^{-3}}{20\times10^{-9}} = 0.5\times10^{6}$$

N = 500,000 clock cycles.