ELEX 2117 : Digital Techniques 2
2021 Winter Term

Flip-Flops and Registers

This lecture is an introduction to flip-flops and registers.
After this lecture you should be able to:

- *convert between high/low logic levels and true/false truth values for active-high and active-low interfaces*
- *predict the relationship between the input and output waveforms of D flip-flops*
- *draw the output waveforms for registers, counter and shift registers*
- *write Verilog descriptions for these*
- *identify specifications on a timing diagram*
- *identify a specification as a requirement or guaranteed response*

Numbers, Logic Levels and Truth Values

Numbers are used for counting, logic levels are voltages, and truth values can be true or false. These are different, but related.

Almost universally, 1 and 0 are synonymous with true and false respectively. But there are two common conventions for the relationship between logic levels and truth values:

Number	Truth	Active High	Active Low
`0`	F	L	H
`1`	T	H	L

Verilog uses the active-high convention: `0` and `1` are treated as low and high respectively.

Active-low signals can be denoted by:

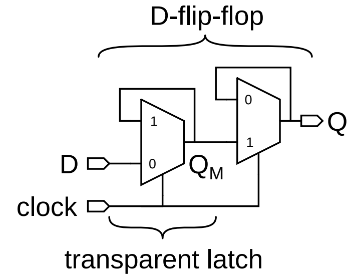
- a bar over the signal name ($\overline{\text{reset}}$)
- an asterisk after the signal name (`RESET*`)
- a suffix of N (or n) after the signal name (`reset_n`)

Exercise 1: Is a signal named $\overline{\textbf{overload}}$ active-high or active-low? Is there an overload if this signal is high? What if the signal was named **overload**?

Exercise 2: Come up with an appropriate name for a signal that is at 3 V when a door is open and 0 V when the door is closed.

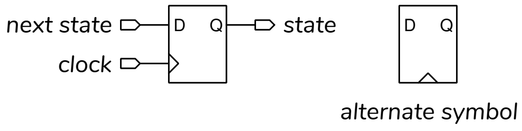
D Flip-Flop

Consider the following circuit composed of two multiplexers:



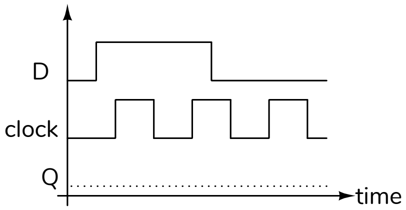
When the clock input is 0, the output of the first multiplexer follows the input – the latch is "transparent". When the clock input is 1, the output level is fed back to the input and held at that level[1].

The symbol for the D flip-flop is:



The rising edge of a clock input causes the flip-flop to store the value of the input and make it available on the output. Thus the D flip-flop has a next-state input (D), a state output (Q) and a clock input. The D flip-flop's state only changes on the rising edge of the clock.

The D flip-flop "stores" one bit and is the memory element used in most sequential logic circuits.

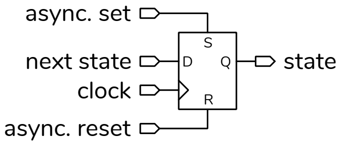


[1] This is a "master-slave" flip-flop. The second, "slave,“ latch holds the previously latched value when the clock is 0

Exercise 3: Fill in the waveform for the **Q** signal in the diagram above.

Asynchronous Inputs

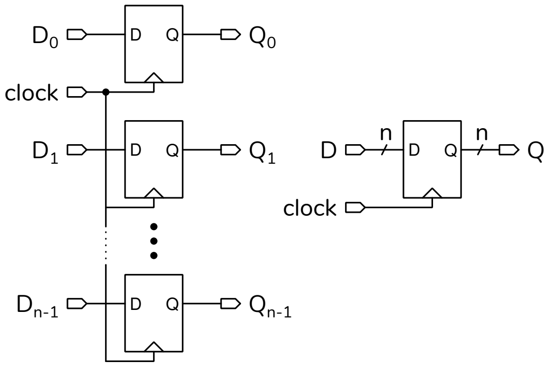
Asynchronous inputs:



can set (to H) or reset (clear to L) the flip-flop state independently of the clock. Ensuring reliable operation of circuits with asynchronous inputs is difficult. Asynchronous inputs are most often used to reset a circuit to a known state when it first powers up or when it fails. We will not use them in this course.

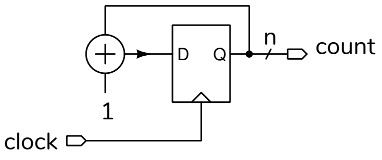
Common Sequential Logic Circuits

Connecting multiple D flip-flops to the same clock so that all are loaded simultaneously creates a *register* . The notation on the right is for a register that is *n* bits wide.

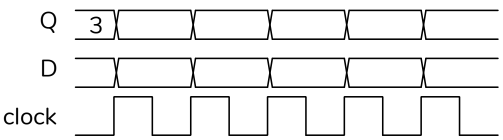


Exercise 4: What would be another name for a 1-bit register?

A *counter* is a register whose value increases by 1 on each rising edge of the clock. It consists of a register whose input is the current value of the counter plus one:



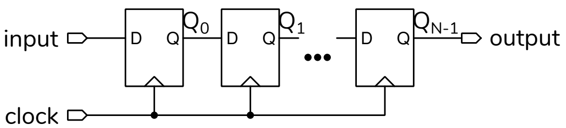
On each clock edge the register loads a value that is one more than the previous value.



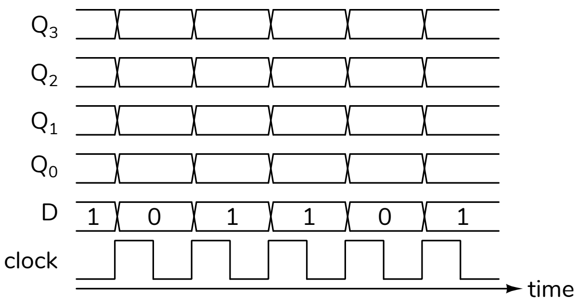
Exercise 5: Assuming a 3-bit counter, fill in the values of D and Q in the diagram above.

Exercise 6: Draw the block diagram for a counter that: (a) counts up by 3? (b) counts down by 1? (c) whose value doubles on each clock edge?

A *shift register* is several registers with the output of each register connected to the input of the next register:



On each rising edge of the clock the state of each register is transferred to the next one.



Exercise 7: Fill in the diagram above for a 4-bit shift register. Assume the initial value of each flip-flop is zero. Which is the oldest (first) value the D waveform? Which flip-flop holds the oldest value?

A shift register makes previous inputs available in parallel. This is useful for detecting sequences and for transferring data serially.

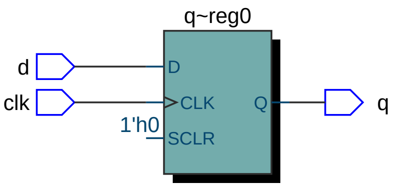
Exercise 8: Add parallel outputs to the shift register schematic. Draw a circuit whose output is high when the sequence 1, 0, 1, 1 is detected. Add the output of this circuit to the timing diagram above.

Registers in Verilog

The following Verilog:

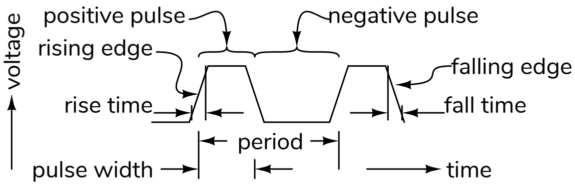
```
module ex2 (input logic d, clk,
            output logic q) ;

   always_ff @(posedge clk)
     q <= d ;

endmodule
```

synthesizes a D-flip-flop that transfers the **d** input to the **q** output on the rising (positive) edge of **clk**:



Exercise 9: What would you change to make an 8-bit register? A 4-bit counter? A 3-bit shift register? Follow the course coding conventions.

Digital Waveforms



A transition from low to high is called a rising edge. The time it takes is called the rise time. A transition from high to low is called a falling edge. The time it takes is called the fall time. Two adjacent edges define a pulse, which can be negative or positive. The time between these is called the pulse width.

Rise and fall times are typically measured between 10% and 90% of the swing. Other measurements are typically made between 50% levels. But there are exceptions.

A signal consisting of periodic pulses is a clock. The inverse of the clock period is the clock frequency.

Timing Specifications

Timing specifications can be:

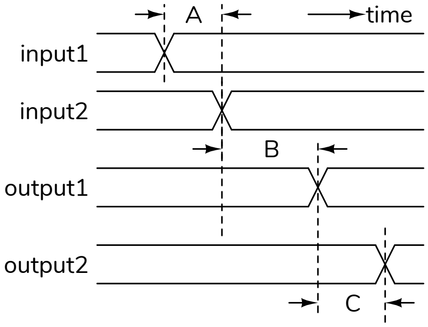
requirements: the manufacturer requires that these specifications be met for a device to operate properly, or

guaranteed responses: the manufacturer guarantees that these specifications will be met.

Since the device manufacturer cannot control the timing on inputs but can guarantee the timing of outputs, a simple rule to distinguish requirements from responses is:

- requirements are measured from a transition on an input *to a transition on an input.*
- guaranteed responses are measured from a transition on an input or an output *to a transition on an output.*

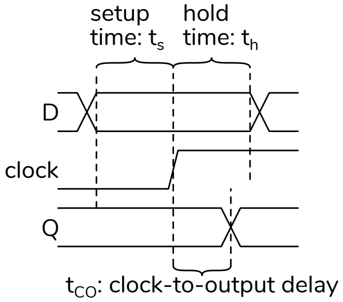
Timing diagrams show the relationship between transitions on inputs and outputs. They are not drawn to scale. Both high and low levels are shown when the specification applies to both.



Exercise 10: Label the specifications A through C as requirements or guaranteed responses.

Combinational logic circuits and D flip-flops have one important timing specification: their propagation delay. This is the delay from a change on an input to the corresponding change on an output. The usual symbols are t_{PD} for propagation delay and t_{CO} for the clock-to-output delay for a D flip-flop.

D flip-flops have two important timing requirements:



setup time the D input must be at a valid logic level for at least t_{S} before the rising edge of the clock

hold time the D input must remain a valid logic level for at least t_{H} after the rising edge of the clock

Timing analysis, be covered later, involves determining whether the timing requirements of the devices in a circuit will be met.