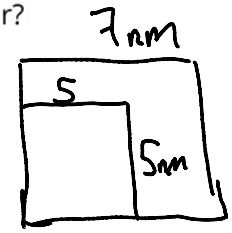
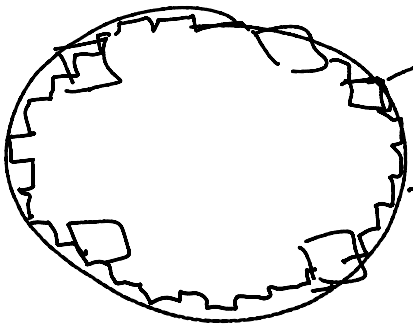
Programmable Logic Applications and Architectures

Exercise 1: What improvement in number of transistors per unit area would be achieved by reducing the transistor dimensions from 7 nm to 5 nm? Approximately how many 5x5 mm die fit on a 300 mm wafer?



$$= \frac{\frac{1}{5nm \times 5nm}}{\frac{1}{7nm \times 7nm}} = \frac{7^2}{5^2} = \frac{49}{25} \simeq 2x$$

doubles # transistor per unit area.



$5 \times 5\,mm = (5 \times 10^{-3})^2$

area $\pi\left(\frac{d}{2}\right)^2 = \pi\left(\frac{0.3}{2}\right)^2$

$$\#\,die \simeq \frac{\left(\frac{\pi}{4}\right) 9 \times 10^{-2}}{25 \times 10^{-6}} = \frac{1}{3} \times 10^4$$

$\simeq$ 3000 die

300 mm
- digital
  - Samsung
  - TSMC
  - Intel → Altera
  - Global Foundries. (AMD) → Xilinx
- memories (SK Hynix, ...)
- analog or mixed-signal (TI, ,)

Exercise 2: Would you use hardware or software to implement: A calculator? A controller for kitchen appliance? An Ethernet interface? To do Bitcoin "mining"?

h/w vs s/w

calculator – s/w

kitchen appliance – microcontroller (s/w)

Ethernet – h/w

Bitcoin mining – h/w

Exercise 3: Would you use a PLD or ASIC for: A project that had to be completed within a month? That would be expected to sell 100 million units? Whose complete requirements aren't known? A state-of-the-art general-purpose CPU?

- 1 month - TTM – PLD
- 100×10^6 – ASIC
- unknown requirements – PLD
- fast CPU - ASIC