Implementation of Digital Logic Circuits

Exercise 1: If $\overline{D}$ is a data bus and $\overline{D0}$ is low, is the value on the data bus an even or odd number?

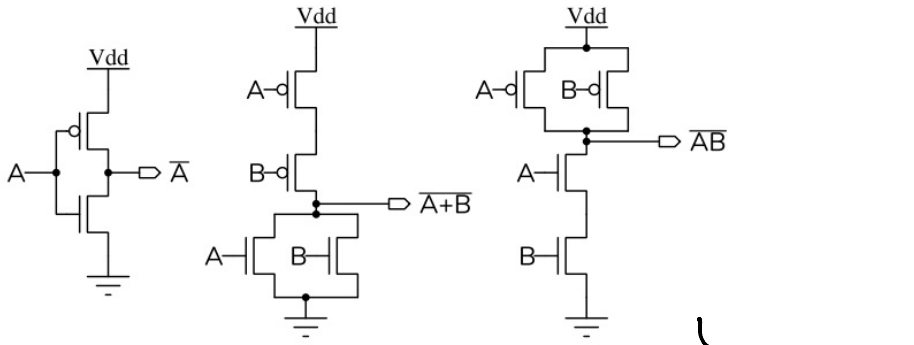
D0 is L.S. bit

$\overline{D0}$ { H = 0, L = 1

$\overline{D0}$ is low → 1

L.S. bit is 1 → odd number

Exercise 2: Which transistors are on when the output is high? When it is low? In which direction does the output current flow in each case?



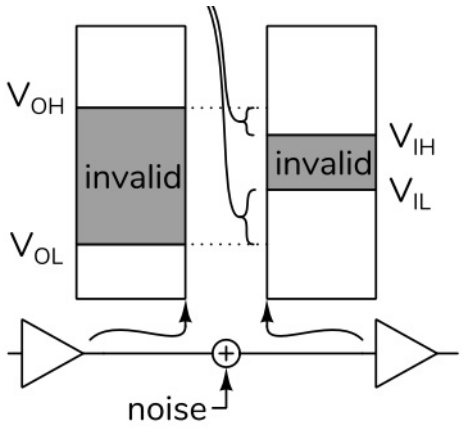
V V

output is high: U is on, h is off — U_0 and U_1 on; h_0 and h_1 off

output is low: U is off, h is on — U_0 or U_1 off; h_0 or h_1 on

Exercise 3: Which of these specifications does the manufacturer guarantee? Which are requirements?

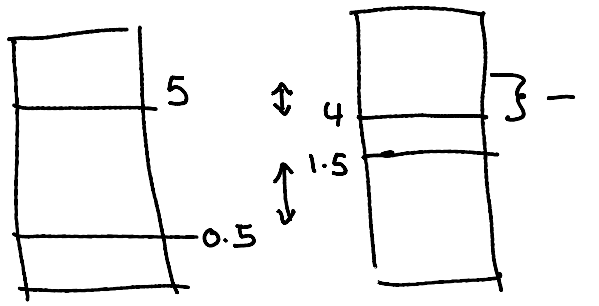
guaranteed (specified) ← output by manuf



→ requirements

Exercise 4: A logic family has ~~V_{OH}~~ V_{OH}(min) = 5 V, ~~V_{OL}~~ V_{OL}(max) = 0.5 V, ~~V_{IH}~~ V_{IH}(min) = 4 V ~~V_{IL}~~ V_{IL} = 1.5 V. What are the noise margins?

V_{IH} V_{IL}



for

H noise marg. $= 5 - 4 = 1V$

L noise margin $= 1.5 - 0.5 = 1V$

Exercise 5: All else being equal, by how much would we expect to decrease power consumption when reducing logic levels from 5 V to 3.3 V? What would be the effect on power consumption in reducing the clock frequency from 50 MHz to 1 MHz?

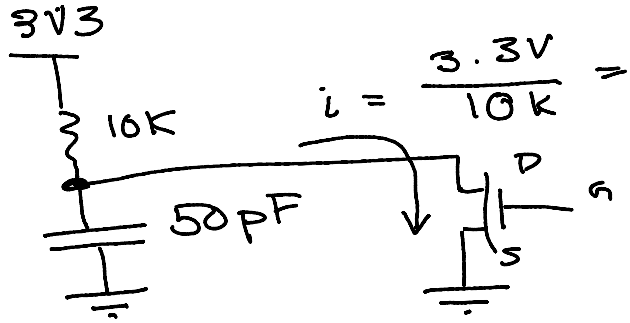
$$P_{5V} = k(5)^2$$

$$P_{3V3} = k(3.3)^2$$

$$\text{ratio} = \frac{P_{3V3}}{P_{5V}} \approx \frac{\cancel{k}\ 11}{\cancel{k}\ 25} \simeq \frac{1}{2}$$

$$\frac{P_{1\,MHz}}{P_{50\,MHz}} = 2\%$$

Exercise 6: What are the active-state current and the RC time constant for a wired-or interrupt-request line using a 10kΩ resistor pulling up a circuit with 50 pF capacitance to 3.3 V?



$$i = \frac{3.3V}{10k} = 0.33\ mA$$

$$\tau = RC = 10 \times 10^3 \cdot 50 \times 10^{-12}$$

$$= 500 \times 10^{-9} = 0.5\ \mu s.$$