Timers and Frequency Dividers

Introduction

Timer circuits measure time by counting clock cycles. Clock dividers, also called frequency dividers, are timer circuits that generate periodic outputs.

In this lab you will use a frequency divider to generate tones by periodically switching the current flowing through a speaker.

The frequency divider's counter counts down from $N-1$ to 0. When the counter reaches zero the output is toggled (changes values). The clock period and N determine the speaker waveform period.

In this lab you will use a 50 MHz clock on the CPLD board. The period of this clock is $1/50\times10^6 = 20$ ns. The period of the speaker waveform is thus $2N \times 20$ ns.

Components

You will need:

- a solderless breadboard
- your EPM240T100C5 CPLD board, Byte Blaster JTAG interface and coaxial power connector,
- a 200 Ω resistor
- two SPST N.O. pushbutton switches (two SPDT switches will also work)
- a speaker
- two cables with alligator clips from your ELEX 1117 parts kit

Specifications

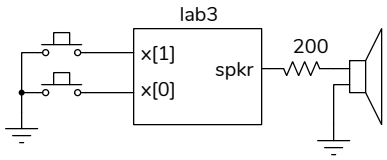
Pushing one or both buttons should result in a tone. The required tone frequencies are determined by your BCIT ID:

right button	$500 + 100d_0$
left button	$500 + 100d_1$
both buttons	$500 + 100d_2$

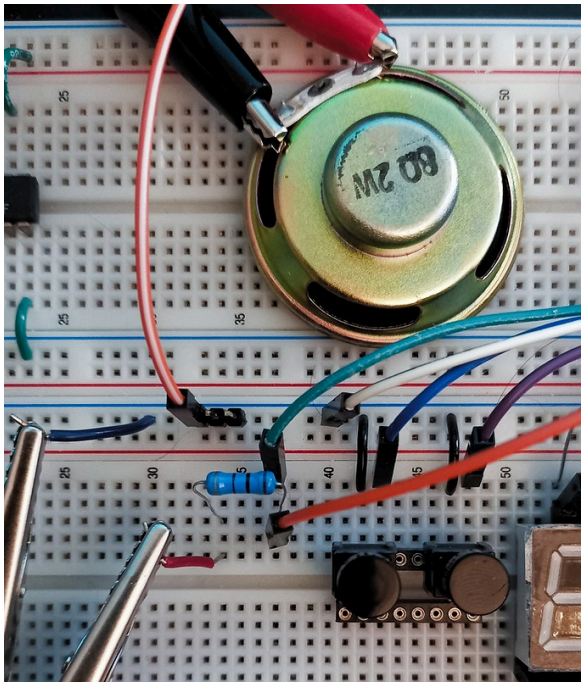
where d_n is the n'th digit of your BCIT ID (n=7 to 0 from left to right). For example, if your BCIT ID was A01234567 the frequencies would be 1200, 1100 and 1000 Hz for the right, left and both buttons respectively.

CPLD I/O

The following diagram shows the connections to the CPLD:



Wire two pushbutton switches and a current-limiting resistor on the breadboard and connect a CPLD I/O pin and the resistor to the speaker with alligator clip cables:



The pin assignments are similar to the previous lab. The n.o. switch inputs are configured with pull-ups and the switch inputs are active-low.

The current-limiting resistor avoids exceeding the maximum current rating of the MAX II CPLD outputs (25 mA)[1]

Sample Design

If no button is being pushed the counter is set to 1. Otherwise if the counter is non-zero, the counter is decremented, otherwise it's loaded with a value equal to the appropriate number of clock cycles for a half period.

The **`speaker`** output is toggled (changed to the opposite value) when the count is **`zero`**. This results in a speaker waveform that is square wave with the required period.

Procedure

Draw a block diagram that implements the circuit described above.

Create a project, compile it, and configure your CPLD. Assign pin 12 to the 50 MHz oscillator input (**`clock`** above).

If you use the same switch pins as in the previous lab and Pin 77 for the speaker output, you should end up with the following assignments:

To	Assignment Name	Value
clk50	Location	PIN_12
x[1]	Location	PIN_99
x[0]	Location	PIN_97
x[0]	Weak Pull-Up Resistor	On
x[1]	Weak Pull-Up Resistor	On
speaker	Location	PIN_77

It's a good idea to assign unused pins as inputs. Under **Assignments** > **Device...** > **Device and Pin Options...** > **Unused Pins** select "As input tri-stated with weak pull-up".

You can download the **`lab3.sdc`** file from the course website and add it to your project (**Project** > **Add/Remove Files in Project...** > **...**) to allow the timing analysis to run without warnings.

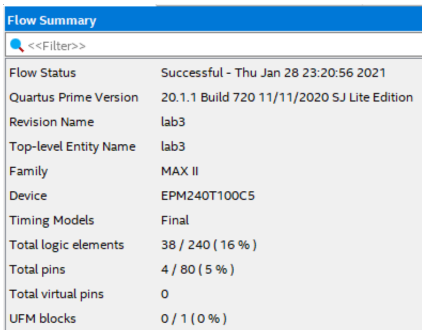
Test your design.

[1]See page 5-1 of the MAX II datasheet available on the course web site.

Submission

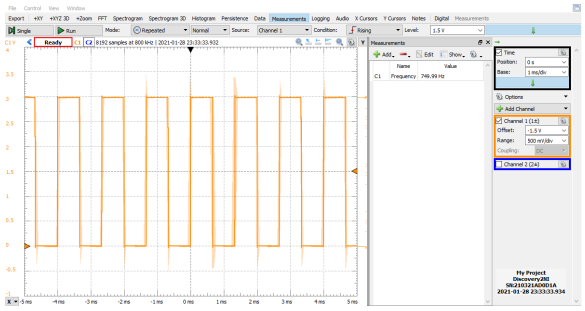
To get credit for completing this lab, submit the following to the Assignment folder for Lab 3 on the course website:

1. A PDF document containing:
   (a) A block diagram of your design.
   (b) A listing of your Verilog code.
   (c) A screen capture of your compilation report (**Window** > **Compilation Report**) similar to this:



Flow Summary	
<<Filter>>	
Flow Status	Successful - Thu Jan 28 23:20:56 2021
Quartus Prime Version	20.1.1 Build 720 11/11/2020 SJ Lite Edition
Revision Name	lab3
Top-level Entity Name	lab3
Family	MAX II
Device	EPM240T100C5
Timing Models	Final
Total logic elements	38 / 240 (16 %)
Total pins	4 / 80 (5 %)
Total virtual pins	0
UFM blocks	0 / 1 (0 %)

   (d) The schematic created by **Tools > Netlist Viewers > RTL Viewer** and then **File > Export...** . The schematic might look like Figure 1.
   (e) A screen capture of the 'scope measurement of the **`speaker`** waveform when both buttons are pushed, including a frequency measurement. This might look like:



2. A short video, including audio, of the tones generated when each combination of pushbuttons is pushed. An example is on the course web site.

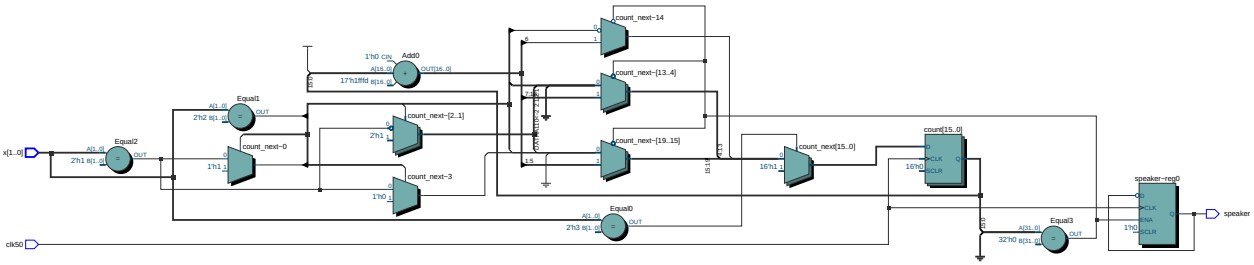


Figure 1: Example RTL Schematic for Lab 3.