ELEX 2117 : Digital Techniques 2
2021 Winter Term

Practice Lab

Introduction

This lab checks that you understand the coding, report formatting and video preparation guidelines. Your mark for this lab will not count.

Block Diagram

Draw a block diagram corresponding to the following Verilog and include it in your report.

```
module sample
  (
   input logic sel,
   input logic [3:0] a, b,
   output logic [3:0] y ) ;

   assign y = sel ? a : b ;

endmodule
```

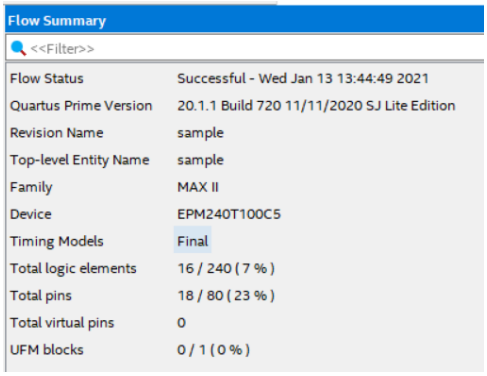
Coding Guidelines

The following Verilog code violates all six of the mandatory coding guidelines. Include a corrected version in your report. The behaviour of the corrected version is immaterial.

```
module sample
  (
    input wire clk, enable,
    output reg [7:0] count, ecount
    ) ;

   always @(posedge clk) begin
      if ( !enable )
        count = count + 1'b1 ;
      end

      always @(posedge enable)
          ecount = ecount + 1'b1 ;

endmodule
```

Screen Capture

Compile the code above using Quartus and include a screen capture of the compilation report (**Window > Compilation Report**) similar to this:



Submissions

Submit the following to the appropriate assignment folder on the course web site before the due date:

- A lab report including the block diagram, corrected code and screen capture described above.
- A 10-second video of your breadboard. The content does not matter.
- The corrected `sample.sv` file (the source code, not a PDF document).