ELEX 2117 : Digital Techniques 2
2020 Winter Term

Solutions to Quiz 2 (second version)

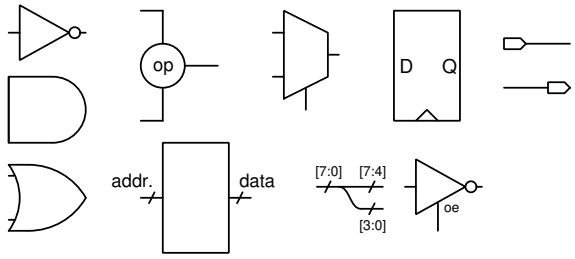
This exam is for the student whose...

surname begins with	BCIT ID ends with

Question	1	2			Total
Mark					
Out of	9	9			18

Question 1: VHDL to Schematic

Using the following schematic symbols:

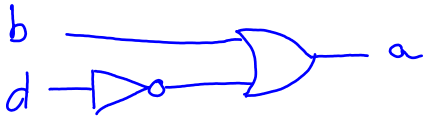


and these declarations:

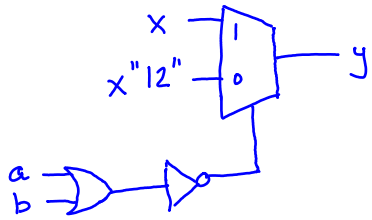
```
type byte_array is array (natural range <>) of
  std_logic_vector(7 downto 0) ;
signal a, b, c, d, w, clk : std_logic ;
signal x, y, z, y_next, n : unsigned (7 downto 0) ;
signal r, s : unsigned (31 downto 0) ;
signal m : byte_array (0 to 3) ;
signal p : unsigned(1 downto 0) ;
```

convert each of the following VHDL expressions into a schematic:

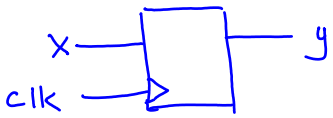
(a) `a <= b or ( not  d ) ;`



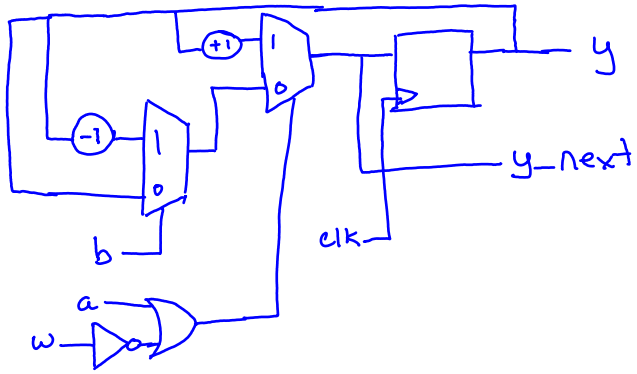
(b) `y <= x when not ( a or b ) else x"12" ;`



(c) `y <= x when rising_edge(clk) ;`



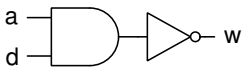
(d)
```
y_next <= y+1 when a = '1' or w = '0' else
          y-1 when b = '1' else
          y ;
y <= y_next when rising_edge(clk) ;
```



Question 2: Schematic to VHDL

Assuming the above signal declarations and schematic symbols, write concurrent VHDL statements that would result in the following schematics:

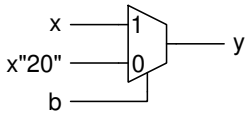
(a)



(a)

```
w <= not ( a and b );
```

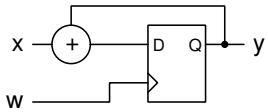
(b)



(b)

```
y <= x when b = '1' else x"20" ;
```

(c)



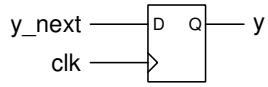
(c)

```
y_next <= y + x ;
y <= y_next when rising_edge(w) ;

OR

y <= y+x when rising_edge(w) ;
```

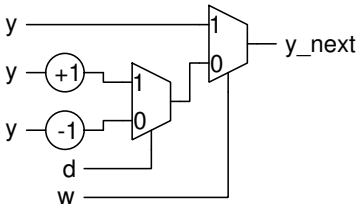
(d)



(d)

```
y <= y_next when rising_edge(clk) ;
```

(e)



(e)

```
y_next <= y when w else
          y+1 when d else
          y-1 ;
```