0

ELEX 2117 : Digital Techniques 2
2020 Winter Term

MIDTERM EXAM 2
1:30 – 2:20 PM
Friday, Feb 28, 2020

This exam has three (3) questions on three (3) pages. The marks for each question are as indicated. There are a total of twenty (20) marks. Answer all questions. Write your answers and all rough work in this paper and nowhere else. Show your work. Draw a box around your final answer. Numerical answers must include units. Books and notes are allowed. No electronic devices other than calculators are allowed. **Show your work.**

This exam paper is for:

Sample Exam 1 A00000000

Each exam is equally difficult.

Answer your own exam.

Do not start until you are told to do so.

Name: _____

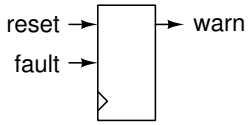
BCIT ID: _____

Signature: _____

Question	Mark	Max.
1		6
2		6
3		8
Total		20

Question 1 — 6 marks

The controller for a warning system:



has one active-high output:

- `warn` that turns on a warning light when it is asserted,

and two active-high inputs:

- `fault` indicates a fault has been detected, and
- `reset` indicates that the warning light should be reset to off.

The controller operates as follows:

- If the reset input is asserted then the warning light should go off.
- If the fault input has been asserted two or more times before the reset input is asserted then the warning light should go on.

You may assume the fault input is synchronized to the clock and lasts exactly one clock period each time it is asserted.

(a) Choose an appropriate number of states and a name for each state.

(b) Draw the state transition diagram. Label each state and draw a directed edge (line with an arrow) between the required state transitions. On each edge write the input condition required for that state condition as an equation (e.g. `reset=1`). The expression must be unambiguous (e.g. a VHDL expression). If there isn't enough space, number the transitions and list the expressions elsewhere.

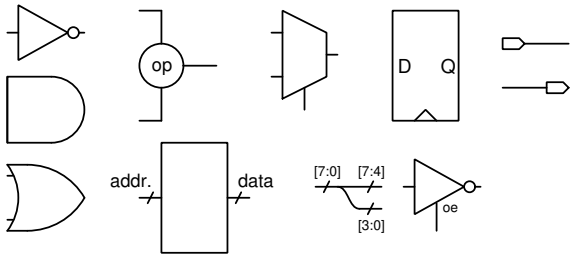
(c) Write expressions for the output as a function of the state and the inputs (e.g. `state=S1`).

Write your answer on the facing page.

Hint: Use the number of faults since the most recent reset as the state.

Question 2 — 6 marks

Using the following schematic symbols and versions with negated inputs and/or outputs:



and these declarations:

```
type byte_array is array (natural range <>) of
  std_logic_vector(7 downto 0) ;
signal a, b, c, d, w, clk : std_logic ;
signal x, y, z, y_next, n : unsigned (7 downto 0) ;
signal r, r_next, s : unsigned (31 downto 0) ;
signal m : byte_array (0 to 3) ;
signal p : unsigned(1 downto 0) ;
```

convert each of the following VHDL expressions into a schematic:

(a)

```
y_next <= y+1 when a = '1' else
     y-1 when b = '1' else
     x"00" when a = '1' and b = '1' else
     y ;

y <= y_next when rising_edge(d) ;
```

(b)

```
a <= b nand c ;
```

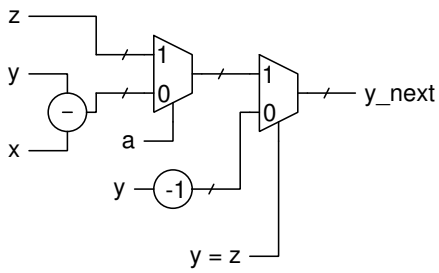
(c)

```
y <= x when a = '1' or b = '1' else
     x"ff" ;
```

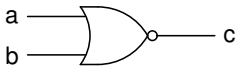
Question 3 — 8 marks

Assuming the previous signal declarations and schematic symbols, write concurrent VHDL statements that would result in the following schematics:

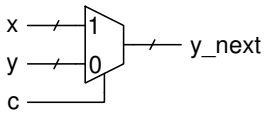
(a)



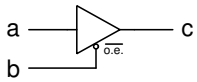
(b)



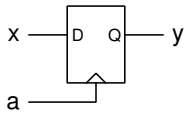
(c)



(d)



(e)



255

ELEX 2117 : Digital Techniques 2
2020 Winter Term

MIDTERM EXAM 2
1:30 – 2:20 PM
Friday, Feb 28, 2020

This exam has three (3) questions on three (3) pages. The marks for each question are as indicated. There are a total of twenty (20) marks. Answer all questions. Write your answers and all rough work in this paper and nowhere else. Show your work. Draw a box around your final answer. Numerical answers must include units. Books and notes are allowed. No electronic devices other than calculators are allowed. **Show your work.**

This exam paper is for:

Sample Exam 2 A00000000

Each exam is equally difficult.

Answer your own exam.

Do not start until you are told to do so.

Name: _____

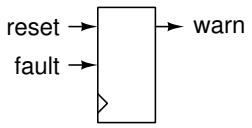
BCIT ID: _____

Signature: _____

Question	Mark	Max.
1		6
2		6
3		8
Total		20

Question 1 — 6 marks

The controller for a warning system:



has one active-high output:

- `warn` that turns on a warning light when it is asserted,

and two active-high inputs:

- `fault` indicates a fault has been detected, and
- `reset` indicates that the warning light should be reset to off.

The controller operates as follows:

- If the reset input is asserted then the warning light should go off.
- If the fault input has been asserted three or more times before the reset input is asserted then the warning light should go on.

You may assume the fault input is synchronized to the clock and lasts exactly one clock period each time it is asserted.

(a) Choose an appropriate number of states and a name for each state.

(b) Draw the state transition diagram. Label each state and draw a directed edge (line with an arrow) between the required state transitions. On each edge write the input condition required for that state condition as an equation (e.g. `reset=1`). The expression must be unambiguous (e.g. a VHDL expression). If there isn't enough space, number the transitions and list the expressions elsewhere.

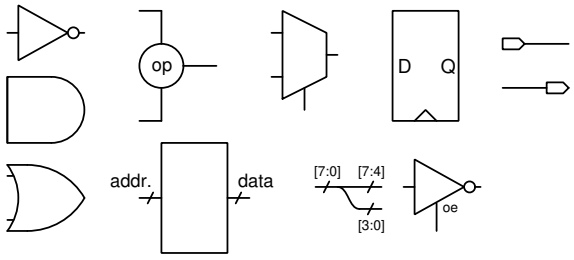
(c) Write expressions for the output as a function of the state and the inputs (e.g. `state=S1`).

Write your answer on the facing page.

Hint: Use the number of faults since the most recent reset as the state.

Question 2 — 6 marks

Using the following schematic symbols and versions with negated inputs and/or outputs:



and these declarations:

```
type byte_array is array (natural range <>) of
  std_logic_vector(7 downto 0) ;
signal a, b, c, d, w, clk : std_logic ;
signal x, y, z, y_next, n : unsigned (7 downto 0) ;
signal r, r_next, s : unsigned (31 downto 0) ;
signal m : byte_array (0 to 3) ;
signal p : unsigned(1 downto 0) ;
```

convert each of the following VHDL expressions into a schematic:

(a)

```
a <= b nand c ;
```

(b)

```
y <= x when a = '1' or b = '1' else
     x"ff" ;
```

(c)

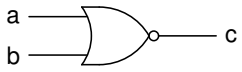
```
y_next <= y+1 when a = '1' else
     y-1 when b = '1' else
     x"00" when a = '1' and b = '1' else
     y ;

y <= y_next when rising_edge(d) ;
```

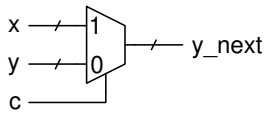
Question 3 — 8 marks

Assuming the previous signal declarations and schematic symbols, write concurrent VHDL statements that would result in the following schematics:

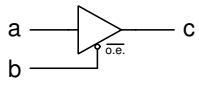
(a)



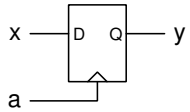
(b)



(c)



(d)



(e)