ELEX 2117 : Digital Techniques 2
2020 Winter Term

Lab Exam Instructions

> This is an examination. Violations of BCIT Policy 5104, "Student Code of Academic Integrity," will be reported. Severe penalties, including suspension, may result.

Introduction

The lab exam requires you to design and implement a state machine using VHDL and your CPLD board.

Each student may be asked to implement a different state machine.

The lab instructor can answer questions about possible ambiguities in the exam and help you resolve problems with the computer hardware. However, he cannot help you complete the exam.

What to Bring

- these instructions
- your BCIT ID (required to hand in your exam)
- your breadboard and CPLD wired and tested as described below
- printouts of lecture notes, labs and any other printed material you think might be useful

The exam is open-book and you may use any printed material or any material stored on a flash drive.

Prohibited Equipment and Network Access

However, all electronic devices other than a calculator and flash drive must be left *at the front of the room*. This includes **cell phones**, laptops[1], tablets, Bluetooth or noise-canceling headsets and smart watches.

The only network access allowed is to the course web site `learn.bcit.ca`. You may only use this web site to download the `labexam.qar` Quartus archive file at the start of the lab and to submit your final `labexam.vhd` file at the end of the lab.

Any other use of the network or possession of a prohibited electronic device will be considered a violation of the BCIT policy on Academic Integrity.

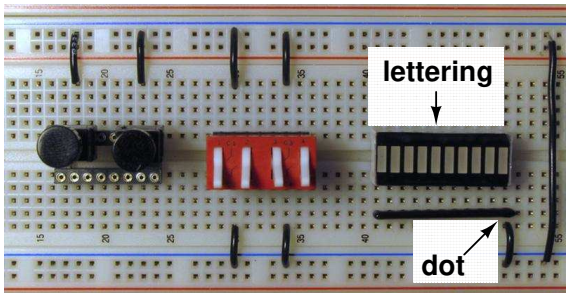
Your use of the lab computer and the network will be monitored and logged.

[1] This means you will not be able to use your own computer for the exam.

Pre-Lab

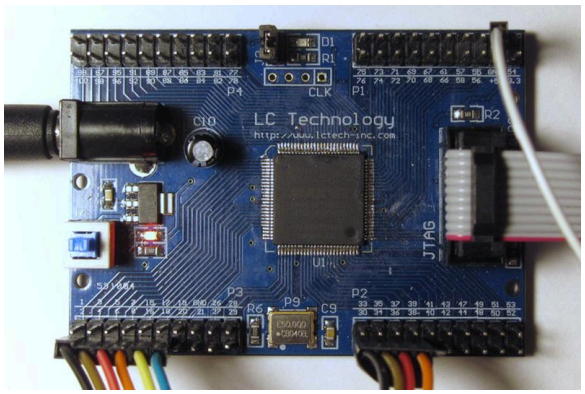
Hardware Configuration

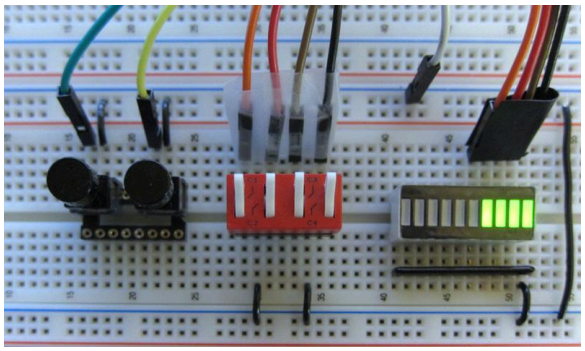
Before the exam you should pre-wire two push-button switches, four toggle switches, a 10-segment LED array and a 10-element resistor array as shown below. Connect the LED array with the anodes (side with lettering) along the top. Ground the end of the resistor array marked with a dot.



Use two wiring harnesses to connect the CPLD board to your breadboard as shown below. Use color coding to keep the wires in order.

Connect the wiring harnesses to your breadboard as shown so that the least-significant bits (black wires) are connected to the bottom left pins (CPLD pins 2 and 30 respectively) of the CPLD pin header connectors P3 and P2 and connect to the rightmost switches and LED segments:





- Use 6 wires for the switch inputs. All will be configured with internal pull-ups.
- Connect the pushbutton inputs to the left contacts as shown; they will be active (high) when pushed.
- Connect the toggle switch inputs to the upper contacts as shown; they will be active (high) when the handle is up.
- Use four wires for the LED outputs.
- The LED outputs will be active (on) when high.
- Connect common (ground, **GND**) from the CPLD to both common (ground) rails on the breadboard.

Hardware Test

Program the CPLD using the **labhwtest.pof** file from the course web site. The red on-board LED displays the exclusive-or of all switch inputs and should change if a pushbutton or toggle switch is pushed or toggled. Pressing the left pushbutton should load the toggle switch values into the LEDs. Each press of the right pushbutton will rotate these values around the display. If you don't see these behaviors then the hardware has not been properly connected.

Inputs and Outputs

For the lab exam you will be supplied with a Quartus project that includes definitions for the switch inputs and LED outputs.

The two pushbuttons inputs are named **l_in** and **r_in** (for the left and right buttons respectively). These are debounced and a rising-edge detector is used to generate the **l** and **r** signals in the architecture. These signals are active high for one clock cycle each time the corresponding button is pushed.

The four toggle switch inputs are named **a** through **d** (from left to right), are not debounced and shouldn't need to be.

The four LED output signals are named **led(3)** through **led(0)** (i.e. **led(3 downto 0)**) in order from left to right.

Your architecture will have available an $\approx$ 1.5 kHz clock named **clk** derived from the on-board 50 MHz oscillator.

Practice Exams

Two practice lab exam worksheets and the **labexam.qar** quartus project archive file are available on the course web site. The format of the worksheets is similar to what will be given to you in the lab exams and the state machines are similar in complexity. You will want to practice doing the practice exams to make sure you are prepared for the exam.

You should also practice downloading and restoring the **labexam.qar** file and uploading your finished **labexam.vhd** file to the appropriate assignment folder on the course web site (Activities / Assignments / Practice Lab Exam VHDL File)[2].

Lab Exam Procedure

Place your BCIT ID on your bench and log in to the course web site.

Design the State Machine

You will be given a worksheet with a state transition diagram showing state names, state transition conditions and outputs for each state. The worksheet will also show a marking table with a sequence of inputs

[2] Make sure you submit to the right folder!

and the expected outputs. The lab instructor will use this table to test your design.

Step 1 Draw a block diagram on the worksheet showing the registers and multiplexers that would implement this state machine, including the correct output for each state. Label the register inputs and outputs and the multiplexer inputs.

Implement the State Machine

Step 2 Create a new folder on the **`D:`** drive named as your surname. Download the **`labexam.qar`** quartus project archive file from the course web site (under Content / Lab Exam) and move it into this folder. Open the **`labexam.qar`** file with Quartus. Extract the archive into the default folder (**`labexam_restored`**). Quartus will recreate the project and open it.

This project is complete except for the details of the architecture. The **`labexam.vhd`** file will have entity and architecture declarations with all required inputs and outputs. All device and pin assignments will have been made. The **`sync_pulse.vhd`** file provides a clock divider, synchronizer, debouncer and pulse generator for your project. The **`labexam.sdc`** file includes timing constraints (you can ignore this file).

Step 3 Follow the course VHDL coding guidelines and add type and signal declarations to the architecture (before **`begin`**) and VHDL code to the architecture (where indicated) that implements your state machine. Add your name in a comment near the top of the file.

Step 4 Compile your design, program the CPLD and check that it works. Fix any errors.

Marking

Twenty minutes before the end of lab exam period – 90 minutes after the start of the exam – you will be told to stop working. You will then have five minutes to...

Step 5 Upload your **`labexam.vhd`** file to the Lab Exam folder on the course web site and leave the room. Late file submissions will not be marked. Leave your BCIT ID, working circuit and worksheet on your bench. The lab instructor will go through the sequence of inputs on your worksheet and assign a mark depending on the number of correct outputs.

The lab exam mark will be computed as follows:

- 50% for working hardware (-10% for each wrong output)
- 25% for handing in a block diagram that matches the state transition diagram (-5% for each missing or incorrect register, multiplexer or signal)
- 25% for submitting reasonably complete VHDL code that conforms to the course coding guidelines. (-5% per missing functionality or significant deviation from the guidelines)