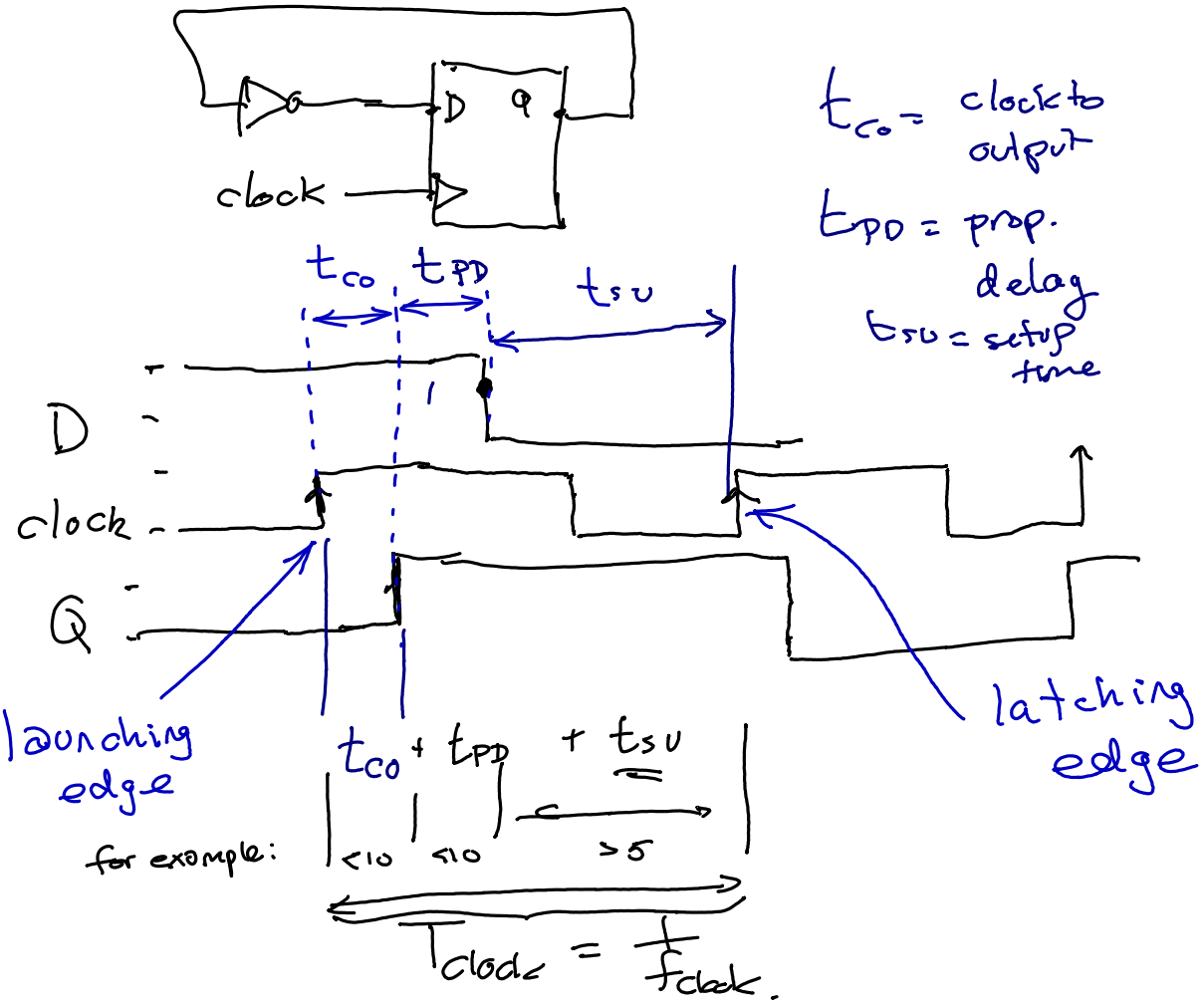
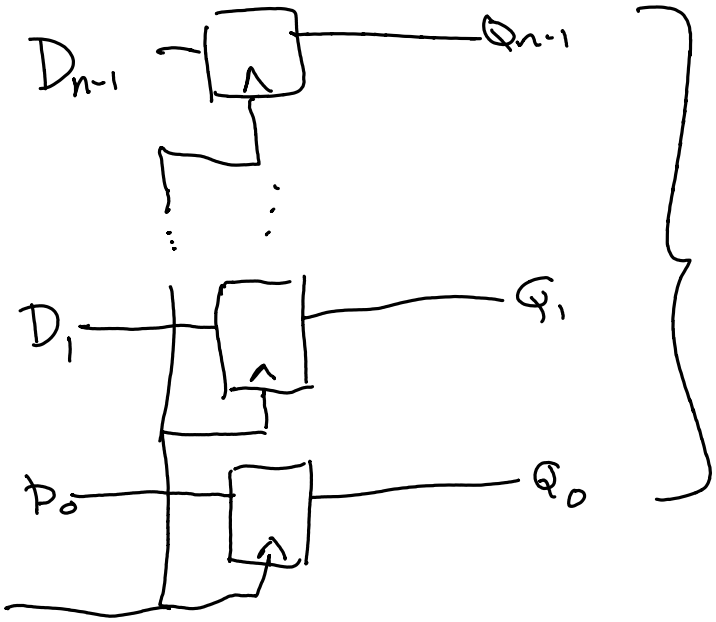
Timing Analysis

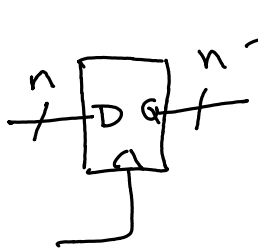


specification	type		measured between
t_{co}	guaranteed (max)	:	input → output
t_{PD}	guaranteed (max)	:	input → output
t_{su}	requirement (min.)	:	input → input

$$\therefore \quad T_{clock}(min) \geq T_{PD}(max) + T_{co}(max) + T_{su}(min)$$

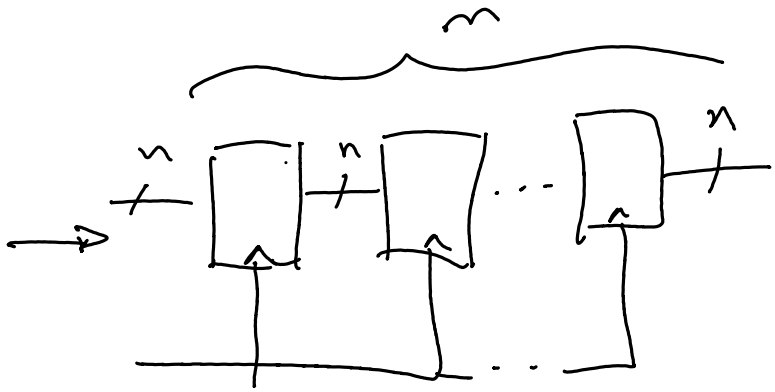
Register : FFs in parallel

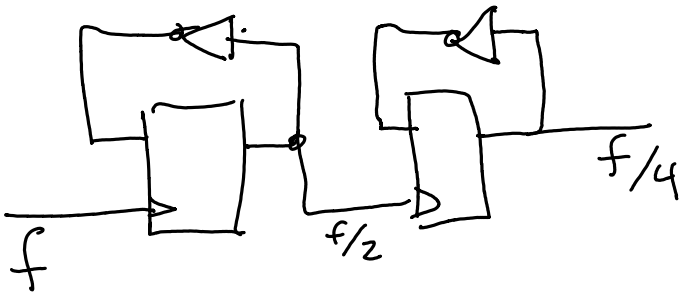




→ means n bits loaded in parallel

Shift Register: FFs in series

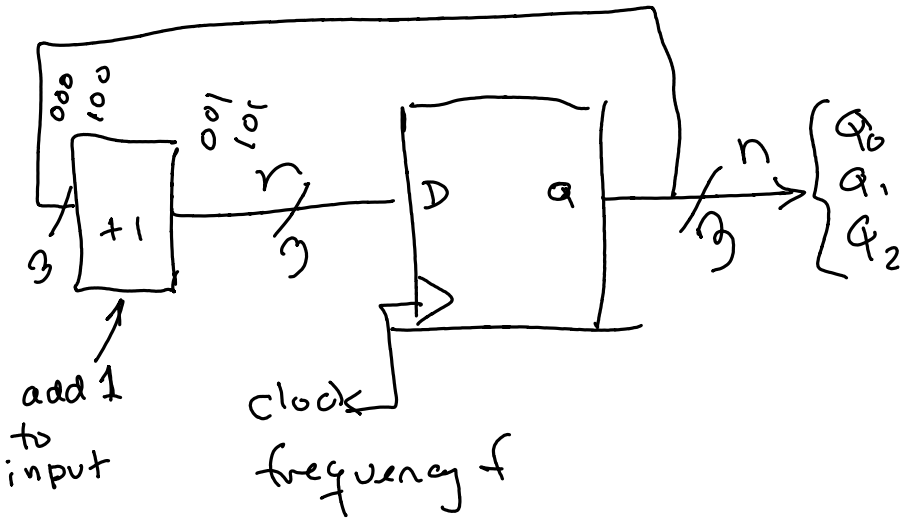




ripple counter (or clock divider). (generally bad)

Synchronous Counter (or clock divider).

(best — all output bits change at same time).



counter values