## Software Installation and Use

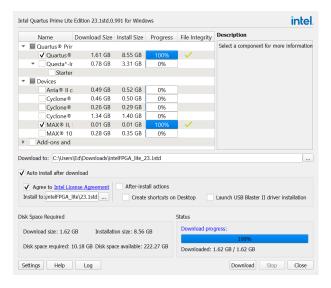
### Installation

## **Quartus and ModelSim**

## **Quartus Prime Lite**

You can run the software from AppsAnywhere or install it locally on your PC. Running Quartus from AppsAnywhere is simpler but may be slower and requires that you be on-line to use the software. Avoid using the same version of Quartus locally that you use from AppsAnywhere – they may conflict.

To install the software locally, download and run the latest Quartus Prime Lite installer from the Intel FPGA Software Download Center. Select the following options:



- under Quartus Prime, select only Quartus Prime (not Questa)
- under Devices, select only MAX II, MAX V device support
- select Auto install after download and Agree to Intel License Agreement
- **unselect** all After-install actions (*important*)

Press Download to download and install the software.

### ModelSim

You'll need to use the ModelSim simulator for one of the labs. If you want to install Modelsim locally, the installer can be downloaded from the Intel website under "Individual Files" for version 20.1. The installer is also available in the ELEX 2117 ShareOut folder. The BCIT ITS Knowledge Base has instructions on accessing ShareIn and ShareOut remotely if necessary. Download and run ModelSimSetup-20.1.1.720-windows.exe, select ModelSim - Intel FPGA Starter Edition (no license required) when installing.

#### **USB-Blaster Driver**

Do *not* install the USB Blaster driver distributed with Quartus. Instead, download the usb-blaster.zip file available on the course website and extract the files. Plug in the USB-Blaster, run Device Manager, and find the USB-Blaster device. Right-click on it and select "Update Driver":



Select the folder where you extracted drivers from the course website. Finally, under Properties / Driver, check that the 2009 driver version was installed:

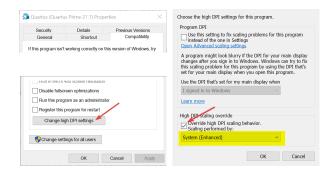


If you have problems when you run the programmer tool, see "Resolving USB-Blaster Problems" below.

There is a short video on the course website showing how to install the software.

# **High-Resolution Displays**

The Quartus user interface may not display properly if you have a high-resolution display and you've set text scaling set to more than 100%. You can work around this by having the operating system scale the Quartus window itself. Right-click the Quartus shortcut and select Properties > Compatibility > Change high DPI settings > High DPI scaling override. Check the Override box and select System (Enhanced):



## **Logic Synthesis with Quartus**

- 1. Run Quartus (on Windows select Intel FPGA ... > Quartus ...).
- 2. Select File > New... > New Quartus Prime Project > OK.
- 3. In the dialog boxes that follow: select a new folder for your lab (e.g. C:\ELEX2117\lab1), enter a project name (e.g. lab1), select an empty project, don't add any files, select the MAX II Family, select the specific device EPM240T100C5, and leave other settings at their defaults.

I recommend putting the project folder on a BCIT network drive (e.g. your Z: drive or BCIT OneDrive) when using the lab computers. This is almost as fast as a local disk. Most flash drives will be slower. Using the D: drive risks other students copying your solution if you forget to delete your files when you leave.

Add any existing design files using Project > Add/Remove Files in Project..., or create new ones using File > New... > System Verilog HDL File. One of

- the files must have a module with the top-level name specified above (in this example, lab1). The port names of this module will correspond to the names assigned to the CPLD pins.
- After all the design files have been created and added to the project, select Processing > Start Compilation. Correct any errors and recompile as necessary.
- 6. Select Assignments > Pin Planner and select the correct pin in the Location drop-down box for each I/O pin. Note that you must compile the project before the pin names are visible in Pin Planner. Recompile the project (Processing > Start Compilation) for the assignments to take effect.
- It's good practice to assign unused pins as inputs. Under Assignments > Device... > Device and Pin Options... > Unused Pins select "As input tri-stated with weak pull-up".
- 8. Connect the CPLD board's coaxial power connector to a USB port and press the power pushbutton so that the power LED lights up.
- Connect the "USB Blaster" to the JTAG port on the CPLD/FPGA board and a free USB port. The POWER and ACT lights on the USB-Blaster should turn on.
- Select Tools > Programmer, click on Hardware Setup..., select USB-Blaster from the drop-down and Close. USB-Blaster should appear next to Hardware Setup...
- 11. If necessary, click on Add File..., navigate to the location of the generated .pof file (typically in the output\_files folder of the project folder) and select the .pof file.
- 12. Check that the Program/Configure checkboxes are checked and press Start to program the device. The progress bar should show 100%.
- 13. Test your design.

There is a short video on the course website showing how to use Quartus to synthesize a design and program a CPLD or FPGA.

## **Quartus Project Files**

Your Quartus project folder will contain:

- a .qpf Quartus Project File that defines the project name and Quartus version
- a .qsf Quartus Settings File with settings including pin assignments and synthesis options
- .sv System Verilog files
- an output\_files folder that contains the .pof Programmer Object Files to program the CPLD

The menu item View > Utility Windows > Project Navigator shows a list of the source files in the project. Many other types of files may also be included in the project folder.

## Simulation with ModelSim

- 1. Run ModelSim (on Windows select Intel FPGA ... > ModelSim ...).
- 2. (a) If this is the first time you simulate this design, select File > New > Project..., select the folder where your files are located as the Project Location, enter a suitable Project Name (e.g. lab1) and click OK. Select Add Existing File and select the file(s) that contain the entities you want to simulate, including your design files and testbench (if any), then select Close.
  - (b) If you had already created a simulation project and it's not already open, select File > Open, select Files of type: Project Files (\*.mpf) and select the project file,
- 3. Select Compile > Compile All to compile all the files in your project into the work library,
- 4. If there are syntax errors you will need to fix the error(s), save the file and go back to step 3,
- 5. Otherwise select Simulate > Start Simulation; select your testbench module from the work library and select **OK**.
- 6. Drag the signals you wish to view from the 'Sim' or 'Object' windows to the 'Wave' window (use the View menu to open windows).

- 7. Select Simulate > Run -All; this will run the simulation until it's complete.
- 8. The Transcript window will contain output from the testbench.
- 9. The Wave window will show the waveforms (select the Wave window, click on '+' and Wave > **Zoom** > Full); you can use a screen capture utility (e.g. Windows Snip tool) to save the waveforms.
- 10. If the results are not as expected, correct the errors, run Compile > Compile All, Simulate > Restart..., click OK and Simulate > Run -All.

## **Resolving USB-Blaster Problems**

If possible, check your USB-Blaster, cables and CPLD or FPGA board at a BCIT lab session by programming one of the .pof files from the course web site. Ask the lab instructor for help if necessary.

If your hardware works with the lab PC but not with your own computer, follow the troubleshooting guide below.

You will need:

- a Windows 10 PC with Quartus Prime installed
- two free USB ports (or one port and one USB charger)
- · a USB flash drive
- (in rare cases) a known-working USB-Blaster, cables, and CPLD or FPGA board

Do the following, in order:

1. Press the **■** (Start) key and type "Core Isolation" or navigate to <sup>™</sup> (Settings) > Update & Security > Windows Security > Device Security and click on Core isolation details.

Check that **Memory Integrity** is set to **Off**:

### Memory integrity

Prevents attacks from inserting malicious code into high-security



The USB-Blaster usblstr.sys drivers are incompatible with Memory integrity protection and will not install if it's enabled.

- 2. Unplug any USB peripherals that are not required to run your computer and restart your computer.
- 3. Check that the flash drive works in the USB port you plan to use for the USB-Blaster. If other devices don't work when plugged into the ports you plan to use, shut down the computer (don't just restart it). If other USB devices still don't work, use a different USB port or computer.
- 4. Disconnect the USB-Blaster from the CPLD/F-PGA board and plug it into the USB port. Check the green POWER LED. If it's not on, try a known-good mini-USB cable and USB-Blaster.
- Run Windows' Device Manager and expand the USB controllers section. You should see the USB-Blaster under Other devices:



### or USB Controllers:



If not, (this is rare) try a known-good mini-USB cable and USB-Blaster.

 Right-click on the USB-Blaster device, select Properties and click on the Driver tab. Check that Driver version 2.4.16.0 is installed as shown below.



if you have a different version then you're probably using the drivers included with Quartus rather than the ones from the course web site. Right-click on Altera USB Blaster and select Uninstall device. *Check the box for Delete the driver software for this device.*<sup>2</sup> and click Uninstall.



If no, or the wrong driver, was installed, install the Altera USB Blaster drivers from the course web site as described above and check the version again. Do not proceed until the correct driver version has been installed.

7. In Quartus, run Tools > Programmer and click on Hardware Setup. Check that you can select the USB-Blaster:



If not, close the programmer application, unplug any USB devices that may be using an FTDI serial interface IC, *including the Analog Discovery 2*, and try again.

If the USB-Blaster shows up in Device manager but the Quartus programmer still cannot detect it, in Device Manager select the USB-Blaster, select Properties and the Driver tab. Click on "Uninstall Device." Then unplug the USB-Blaster and plug it in again. This should cause the driver to be reloaded and the USB-Blaster to re-appear in Device Manager.

If the USB-Blaster shows up in Device manager but the Quartus programmer still cannot detect it, go to step 1 (and make sure all USB devices are unplugged before restarting).

8. At this point the USB-Blaster should still be disconnected from the CPLD/FPGA board. Remove all connections to the CPLD/FPGA pins (to prevent issues due to short-circuited pins) and connect the micro-USB power connector to a USB power supply or USB port. If the

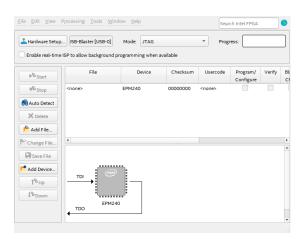
<sup>&</sup>lt;sup>1</sup>USB port power is turned off when you draw too much current (e.g. due to a short circuit on your breadboard).

 $<sup>^2</sup>$ You must delete the newer driver so it does not get reinstalled.

red power LED does not light, check the USB port/charger and cable. Replace the micro-USB cable or CPLD/FPGA board if the power LED does not light.

**Note:** The USB-Blaster supplies enough power to light the red power LED on the CPLD/F-PGA board but not enough for the CPLD/F-PGA to operate. Do not rely on the power LED on the CPLD/FPGA board to show whether the CPLD/FPGA is receiving power.

- 9. Connect the USB-Blaster to the CPLD/FPGA board's JTAG connector using the ribbon cable. Note that the connectors are keyed.
- 10. Click on **Auto Detect** to check that the device is detected:



- 11. If the device is not detected you should see a pop-up message saying "Unable to scan device chain." Run Tools > JTAG Chain Debugger or Click Yes if the message offers to run it for you.
- 12. Click on Test JTAG Chain.

If the error is "Chain is in use." reboot the computer to restart the USB-Blaster driver.

If the error is "No device detected." double-check the connection between the USB-Blaster and the CPLD/FPGA board. Replace the USB-Blaster, ribbon cable, or CPLD/FPGA board<sup>3</sup>.

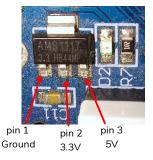
# **Troubleshooting the Hardware**

If substituting known-good hardware shows that the problem is with your CPLD/FPGA board or USB-Blaster some additional checks may confirm the fault. In most cases the problem will be with a power supply or I/O pin.

Schematics for the CPLD/FPGA board and the USB-Blaster are available on the course website if you want to do additional troubleshooting.

## **CPLD Board**

Disconnect everything from the header pins and the USB-Blaster from the JTAG port. Connect the power connector to a USB port and measure the voltages on the AMS1117 voltage regulator pins:



If pin 3 reads 5 V but pin 2 (center pin) is not at 3.3 V then check for a shorted power rail (from pin 2 to ground). Otherwise, the regulator may have failed. Power the board from an external 3.3 V supply using the pins labelled GND and +3.3 at the top right of the board. Limit the current to avoid burning up failed components.

### **USB-Blaster**

There aren't many components in the STM-32-based ("clone") USB-Blaster. You can remove the top cover:



and check for 3.3 VDC between the USB shield and the heat sink tab on the voltage regulator (U4). On the bottom of the board you'll find ground and 3.3 VDC supplied from the FPGA board.

<sup>&</sup>lt;sup>3</sup>Although the most common reason for this error is that there is no power connected to the CPLD/FPGA board.