Solutions to Quiz 3

There were two versions of each question. The values and the answers for both versions are given below.

Question 1

A TTL logic gate has V_{OH}=2.7 (or 2.4) V and V_{IH}=2 V. A CMOS logic gate has V_{OH}=2.4 V and V_{IH}=2 V.

(a) What is the (high-level) noise margin for a CMOS output driving a TTL input?

(b) What is the (high-level) noise margin for a TTL output driving a CMOS input?

Answers

The high-level noise margin is $V_{OH} - V_{IH}$.

(a) For a CMOS output and TTL input the noise margin is $2.4 - 2 = \boxed{0.4\,\text{V}}$.

(b) For a TTL output and a CMOS input the noise margin is $2.7 - 2 = \boxed{0.7\,\text{V}}$ (or $2.4 - 2 = \boxed{0.4\,\text{V}}$).

Question 2

What clock rate would be required by a PWM DAC with 8 (or 6)-bit resolution and a 10 kHz pulse rate?

Answers

For a PWM DAC the clock rate is 2^n times the pulse rate where n is the number of bits of resolution. The required clock rate is thus $2^8 \times 10\,\text{kHz} = \boxed{2.56\,\text{MHz}}$ (or $2^6 \times 10\,\text{kHz} = \boxed{640\,\text{kHz}}$).

Question 3

A sine wave with an amplitude of 2 (or 3) V is sampled using a 6-bit A/D converter. What is the power of the quantization noise? Assume the resistance is 1 Ω. Give your answer in Watts.

Hints: (1) The power of a sine wave of amplitude A is $A^2/2$ (for $R = 1\,\Omega$). (2) The ratio of the powers S and N in dB is $10\log(\frac{S}{N})$.

Answers

The power of the sine wave is $S = V^2/2 = 2^2/2 = 2\,\text{W}$ (or $S = V^2/2 = 3^2/2 = 4.5\,\text{W}$).

For B = 10-bit ADC the quantization SNR is $1.76 + 6B = 61.76\,\text{dB}$. The ratio in linear units is $S/N = 10^{61.76/10}$.

Solving for the noise power, $N \approx 2/10^{61.76/10} \approx \boxed{1.33 \times 10^{-6}\,\text{W}}$ (or $4.5/10^{61.76/10} \approx \boxed{3.00 \times 10^{-6}\,\text{W}}$).

Question 4

Which of the following changes would most reduce power consumption?

- reduce the supply voltage to 1/2 (or 1/3) of the original, or
- reduce the clock rate to 1/3 (or 1/10) of the original

Justify your answer.

Answers

(1) Reducing the supply voltage to 1/2 of the original results in a power consumption of $P_2/P_1 = (V_2/V_1)^2 = (1/2/1)^2 = 1/4$ while reducing the clock rate to 1/3 of the original results in a power consumption of $P_2/P_1 = f_2/f_1 = 1/3$.

Since 1/4 is less than 1/3, $\boxed{\text{reducing the supply voltage}}$ most reduces power consumption.

(2) Reducing the supply voltage to 1/3 of the original results in a power consumption of $(1/3/1)^2 = 1/9$ while reducing the clock rate to 1/10 of the original results in a power consumption of $P_2/P_1 = f_2/f_1 = 1/10$

Since 1/9 is greater than 1/10, $\boxed{\text{reducing the frequency}}$ most reduces power consumption.