ELEX 2117 : Digital Techniques 2
2024 Fall Term

Quiz 3
9:30 AM – 10:20 AM
Wednesday, November 20, 2024
SW01-1025

This exam has four (4) questions on one (1) pages. The marks for each question are as indicated. There are a total of eleven (11) marks. Answer all questions. Write your answers and all rough work in this paper and nowhere else. Show your work. Underline or draw a box around your final answer. Numerical answers must include units. Books and notes are allowed. No electronic devices other than calculators are allowed. **Show your work.**

This exam paper is for:

Paper, Test 1 A00123456

Each exam is equally difficult.

Answer your own exam.

Do not start until you are told.

Name: _____

BCIT ID: _____

Signature: _____

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Question 1 — 4 marks

A TTL logic gate has V_{OH}=2.4 V and V_{IH}=2 V. A CMOS logic gate has V_{OH}=2.4 V and V_{IH}=2 V.

(a) What is the (high-level) noise margin for a CMOS output driving a TTL input?

(b) What is the (high-level) noise margin for a TTL output driving a CMOS input?

Question 2 — 2 marks

What clock rate would be required by a PWM DAC with 6-bit resolution and a 10 kHz pulse rate?

Question 3 — 3 marks

A sine wave with an amplitude of 3 V is sampled using a 10-bit A/D converter. What is the power of the quantization noise? Assume the resistance is 1 Ω. Give your answer in Watts.

Hints: (1) The power of a sine wave of amplitude A is $A^2/2$ (for $R = 1\,\Omega$). (2) The ratio of the powers S and N in dB is $10\log(\frac{S}{N})$.

Question 4 — 2 marks

Which of the following changes would most reduce power consumption?

- reduce the supply voltage to 1/3 of the original, or
- reduce the clock rate to 1/10 of the original

Justify your answer.

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Question 1 — 4 marks

A TTL logic gate has V_{OH}=2.7 V and V_{IH}=2 V. A CMOS logic gate has V_{OH}=2.4 V and V_{IH}=2 V.

(a) What is the (high-level) noise margin for a CMOS output driving a TTL input?

(b) What is the (high-level) noise margin for a TTL output driving a CMOS input?

Question 2 — 2 marks

What clock rate would be required by a PWM DAC with 8-bit resolution and a 10 kHz pulse rate?

Question 3 — 3 marks

A sine wave with an amplitude of 2 V is sampled using a 10-bit A/D converter. What is the power of the quantization noise? Assume the resistance is 1 Ω. Give your answer in Watts.

Hints: (1) The power of a sine wave of amplitude A is $A^2/2$ (for $R = 1\,\Omega$). (2) The ratio of the powers S and N in dB is $10\log(\frac{S}{N})$.

Question 4 — 2 marks

Which of the following changes would most reduce power consumption?

- reduce the supply voltage to 1/2 of the original, or
- reduce the clock rate to 1/3 of the original

Justify your answer.