ELEX 2117 : Digital Techniques 2
2024 Fall Term

Quiz 2
9:30 AM – 10:20 AM
Wednesday, October 15, 2024
SW01-1025

This exam has three (3) questions on two (2) pages. The marks for each question are as indicated. There are a total of eighteen (18) marks. Answer all questions. Write your answers and all rough work in this paper and nowhere else. Show your work. Underline or draw a box around your final answer. Numerical answers must include units. Books and notes are allowed. No electronic devices other than calculators are allowed. **Show your work.**

This exam paper is for:

Paper, Test 1 A00123456

Each exam is equally difficult.

Answer your own exam.

Do not start until you are told.

Name: _____

BCIT ID: _____

Signature: _____

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Question 1 — 2 marks

Fill the table below with the value of each expression as a Verilog numeric literal including the correct width and the correct value in *hexadecimal* base. Assume the following declarations:

```
logic [7:0] x ;
logic [3:0] y ;
```

and that `x` has the value `8'hA6` and that `y` has the value `4'b0101`. The first row has been filled in as an example. You need not show your work or draw another box around the answer

expression	value
`x[3:0]`	`4'h6`
`{ x >> 4, y == 5 }`	
`x ^ y ^ x + 1`	

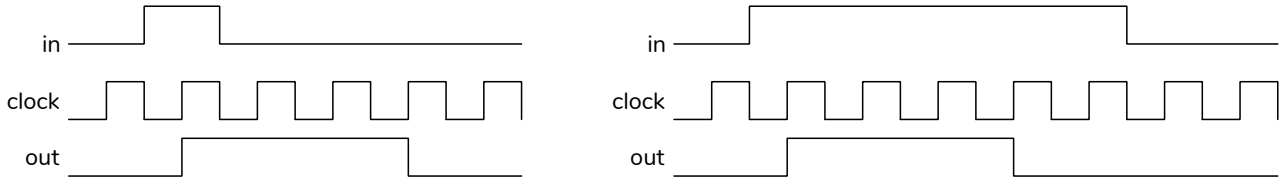
Question 2 — 2 marks

A digital circuit using a 100 MHz clock generates a 20 ms delay by decrementing a counter once per clock cycle. The count starts at $N - 1$ and reaches 0. What is N? Show your work.

Question 3 — 14 marks

A "pulse width normalizer" circuit has two one-bit inputs named **`reset`** and **`in`**, a one-bit output named **`out`**, and a clock. It is a Moore state machine: the output only changes on the rising edge of the clock. The circuit outputs pulses with a duration of three clock periods for every input pulse.

The following diagrams show examples of the required behaviour when the **`in`** pulse is shorter than 3 clock periods and when the **`in`** pulse is longer than 3 clock periods:

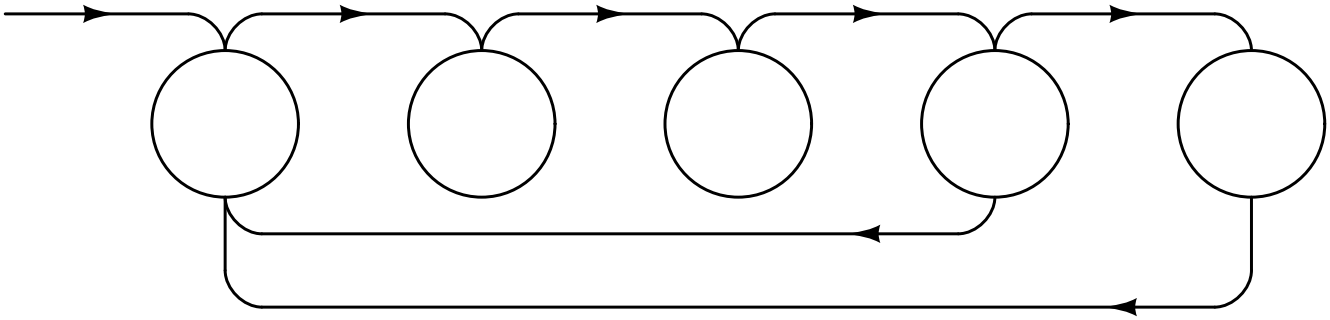


The output behaves as follows:

1. if **`reset`** is high (1) then **`out`** goes low (0), otherwise
2. while **`in`** is low, **`out`** stays low,
3. when **`in`** goes high, **`out`** goes high for exactly three clock periods, even if **`in`** goes low during that time,
4. after the output pulse:
    - if **`in`** is low, **`out`** goes low until **`in`** goes **`hi`** again (as in 2 above), otherwise
    - if **`in`** is high, **`out`** goes low and remains low until **`in`** has gone low and then stays low until **`in`** goes **`hi`** again (as in 2 above),

You may ignore cases where the input pulse duration is less than one clock period or where the time between input pulses is less than five clock periods.

The state transition diagram below implements this state machine. Fill in the circles that describe each state and label the edge (arrows) with the state transition conditions. Follow the conventions used in the lecture notes. Use a **binary** encoding for the states.



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Question 1 — 2 marks

Fill the table below with the value of each expression as a Verilog numeric literal including the correct width and the correct value in *hexadecimal* base. Assume the following declarations:

```
logic [7:0] x ;
logic [3:0] y ;
```

and that `x` has the value `8'h38` and that `y` has the value `4'b0101`. The first row has been filled in as an example. You need not show your work or draw another box around the answer

expression	value
`x[3:0]`	`4'h8`
`{ x >> 4, y == 5 }`	
`x ^ y ^ x + 1`	

Question 2 — 2 marks

A digital circuit using a 100 MHz clock generates a 10 ms delay by decrementing a counter once per clock cycle. The count starts at $N - 1$ and reaches 0. What is N? Show your work.

Question 3 — 14 marks

A "pulse width normalizer" circuit has two one-bit inputs named **`reset`** and **`in`**, a one-bit output named **`out`**, and a clock. It is a Moore state machine: the output only changes on the rising edge of the clock. The circuit outputs pulses with a duration of three clock periods for every input pulse.

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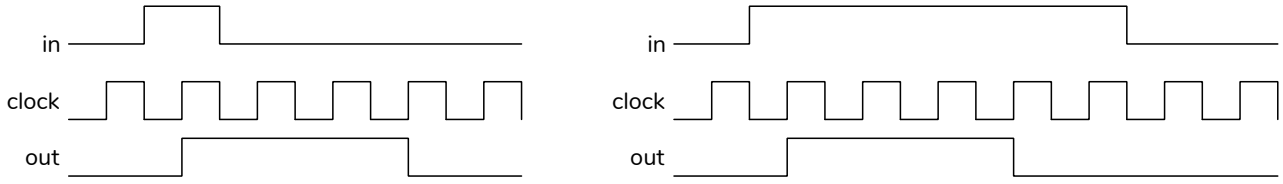

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You may ignore cases where the input pulse duration is less than one clock period or where the time between input pulses is less than five clock periods.

The state transition diagram below implements this state machine. Fill in the circles that describe each state and label the edge (arrows) with the state transition conditions. Follow the conventions used in the lecture notes. Use a **one-hot** encoding for the states.