Solutions to Quiz 1

There were two versions of each question. The values and the answers for both versions are given below.

Question 1

Fill the table below with the value of each expression as a Verilog numeric literal including the correct width and the correct value in *hexadecimal* base. Assume the following declarations:

```
logic [7:0] x ;
logic [3:0] y ;
```

and that `x` has the value `8'h38` (or `8'hA6`) and that `y` has the value `4'b0101`. The first row has been filled in as an example. You need not show your work or draw another box around the answer

Answers

For `x=8'h38` and `y=4'b0101`:

expression	value
x[3:0]	4'h8
x[2:1]	2'h0
!x	1'h0
x[3:0] + x[6:4]	4'hb
x >> 4 ^ y	8'h6
x & y + 1	32'h0
{ x[7:4], x >> 4 }	12'h303
(3'b100+3'b100)*4'b1	4'h8
x ^ x ? x : y	8'h5

and for `x=8'ha6` and `y=4'b0101`:

expression	value
x[3:0]	4'h6
x[2:1]	2'h3
!x	1'h0
x[3:0] + x[6:4]	4'h8
x >> 4 ^ y	8'hf
x & y + 1	32'h6
{ x[7:4], x >> 4 }	12'ha0a
(3'b100+3'b100)*4'b1	4'h8
x ^ x ? x : y	8'h5

Question 2

Write a Verilog module named `compare` that has two 16-bit logic inputs named `a` and `b`, and a `logic` output named `gt` (or `lt`). The value of this output should be set to `1` if `a` is `greater` (or `less`) that `b`, and `0` otherwise. Declare arrays in decreasing bit order. Follow the course coding guidelines but omit comments.

Answers

```
module compare_
  ( input logic [15:0] a, b,
    output logic lt ) ;

   assign lt = a < b ;

endmodule

module compare
  ( input logic [15:0] a, b,
    output logic gt ) ;

   assign gt = a > b ;

endmodule
```

From which Quartus generates the following schematics: