ELEX 2117 : Digital Techniques 2
2024 Fall Term

Quiz 1
9:30 AM – 10:20 AM
Wednesday, September 18, 2024
SW01-1021

This exam has two (2) questions on two (2) pages. The marks for each question are as indicated. There are a total of eleven (11) marks. Answer all questions. Write your answers and all rough work in this paper and nowhere else. Show your work. Underline or draw a box around your final answer. Numerical answers must include units. Books and notes are allowed. No electronic devices other than calculators are allowed. **Show your work.**

This exam paper is for:

Paper, Test 1 A00123456

Each exam is equally difficult.

Answer your own exam.

Do not start until you are told.

Name: _____

BCIT ID: _____

Signature: _____

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Question 1 — 8 marks

Fill the table below with the value of each expression as a Verilog numeric literal including the correct width and the correct value in *hexadecimal* base. Assume the following declarations:

```
logic [7:0] x ;
logic [3:0] y ;
```

and that `x` has the value `8'hA6` and that `y` has the value `4'b0101`. The first row has been filled in as an example. You need not show your work or draw another box around the answer

expression	value
`x[3:0]`	`4'h6`
`x[2:1]`	
`!x`	
`x[3:0] + x[6:4]`	
`x >> 4 ^ y`	
`x & y + 1`	
`{ x[7:4], x >> 4 }`	
`(3'b100+3'b100)*4'b1`	
`x ^ x ? x : y`	

Question 2 — 3 marks

Write a Verilog module named `compare` that has two 16-bit `logic` inputs named `a` and `b`, and a `logic` output named `lt`. The value of this output should be set to `1` if `a` is less than `b`, and `0` otherwise. Declare arrays in decreasing bit order. Follow the course coding guidelines but omit comments.

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Question 1 — 8 marks

Fill the table below with the value of each expression as a Verilog numeric literal including the correct width and the correct value in *hexadecimal* base. Assume the following declarations:

```
logic [7:0] x ;
logic [3:0] y ;
```

and that `x` has the value `8'h38` and that `y` has the value `4'b0101`. The first row has been filled in as an example. You need not show your work or draw another box around the answer

expression	value
`x[3:0]`	`4'h8`
`x[2:1]`	
`!x`	
`x[3:0] + x[6:4]`	
`x >> 4 ^ y`	
`x & y + 1`	
`{ x[7:4], x >> 4 }`	
`(3'b100+3'b100)*4'b1`	
`x ^ x ? x : y`	

Question 2 — 3 marks

Write a Verilog module named `compare` that has two 16-bit `logic` inputs named `a` and `b`, and a `logic` output named `gt`. The value of this output should be set to `1` if `a` is greater than `b`, and `0` otherwise. Declare arrays in decreasing bit order. Follow the course coding guidelines but omit comments.