ELEX 2117 : Digital Techniques 2
2024 Fall Term

MIDTERM EXAM 2

15:30-18:20
Friday, November 1, 2024
SW01-1021

This exam has five (5) questions on two (2) pages. The marks for each question are as indicated. There are a total of seventeen (17) marks. Answer all questions. Write your answers and all rough work in this paper and nowhere else. Show your work. Underline or draw a box around your final answer. Numerical answers must include units. Books and notes are allowed. No electronic devices other than calculators are allowed. **Show your work.**

This exam paper is for:

Sample Exam 1 A00123456

Each exam is equally difficult.

Answer your own exam.

Do not start until you are told.

Name: _____

BCIT ID: _____

Signature: _____

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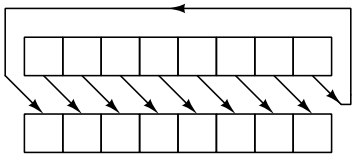
Question 1 — 3 marks

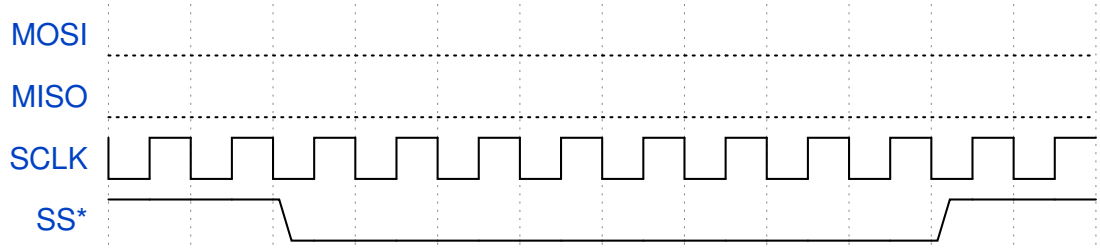
Write *one* System Verilog statement that implements an 8-bit register named `rr` that *rotates* its contents right when a `rot` signal is asserted (true). Rotate means that the contents of the register are shifted right and the rightmost bit is shifted in on the left as shown in the following diagram:



Do not include a module definition. You can assume that `rr` has been declared as `logic [7:0] rr`, that `rot` has been declared as `logic rot`, and that there is a clock signal named `clk`. Follow the course coding guidelines but omit comments.

Question 2 — 4 marks

The diagram below shows the waveforms of an SPI interface that follows the conventions described in the lecture notes. Fill in *one* of the two missing waveforms so that the 8-bit value 8'h72 is transferred from the **master to the slave**. *Note: No marks will be awarded if you fill in both waveforms.*



Question 3 — 4 marks

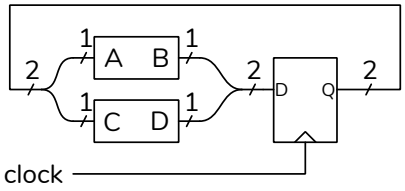
Write System Verilog statements to be placed at the top level of a testbench module to wait until the variable `clkcnt` is equal to 8000and then print the string `Simulation Complete` and end the simulation.

Write only the statements required to accomplish this, not the complete testbench. You may assume `clkcnt` has been declared as `integer clkcnt`.

Hint: "top level" means not *inside an* `initial` *or* `always` *block.*

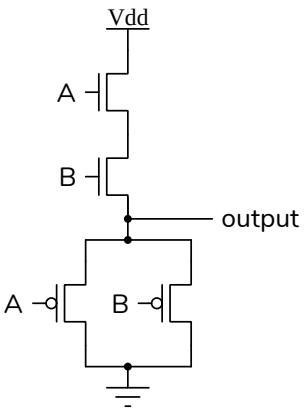
Question 4 — 4 marks

The digital circuit below has a 2-bit register with a minimum setup time requirement of 10 ns. The combinational logic path from A to B has a (maximum) delay of 10 ns. The combinational logic path from C to D has a (maximum) delay of 20 ns. The register's clock-to-output delay is 5 ns (maximum). What is the maximum clock *frequency* at which this circuit will operate reliably?



Question 5 — 2 marks

What logic function of the inputs A and B does the following schematic implement? *Briefly* explain your reasoning or show how you obtained your answer. *Hint1: The arrangement of the N- and P-channel MOSFETs is reversed from the NAND and NOR gates in the lecture notes. Hint2: Work out which transistors are on and which are off for all four possible input combinations.*



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This exam paper is for:

Sample Exam 2 A01234567

Each exam is equally difficult.

Answer your own exam.

Do not start until you are told.

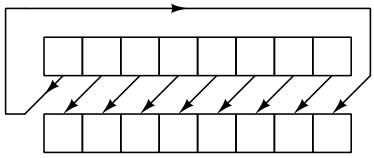
Name: _____

BCIT ID: _____

Signature: _____

Question 1 — 3 marks

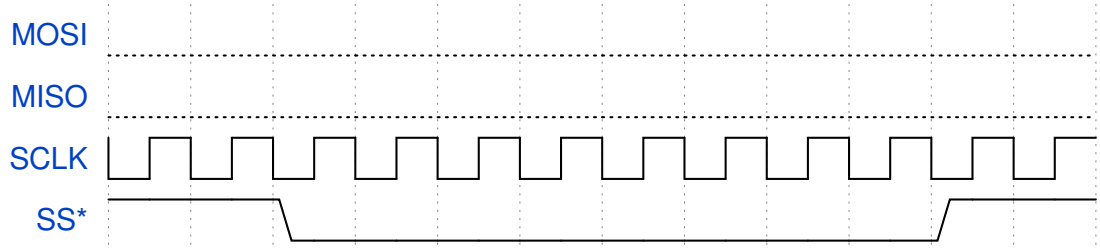
Write *one* System Verilog statement that implements an 8-bit register named **`rr`** that *rotates* its contents left when a **`rot`** signal is asserted (true). Rotate means that the contents of the register are shifted left and the leftmost bit is shifted in on the right as shown in the following diagram:



Do not include a module definition. You can assume that **`rr`** has been declared as **`logic [7:0] rr`**, that **`rot`** has been declared as **`logic rot`**, and that there is a clock signal named **`clk`**. Follow the course coding guidelines but omit comments.

Question 2 — 4 marks

The diagram below shows the waveforms of an SPI interface that follows the conventions described in the lecture notes. Fill in *one* of the two missing waveforms so that the 8-bit value `8'hb1` is transferred from the **slave to the master**. *Note: No marks will be awarded if you fill in both waveforms.*



Question 3 — 4 marks

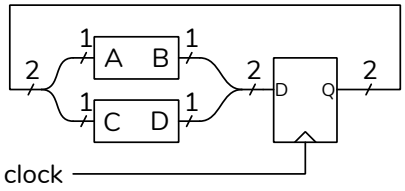
Write System Verilog statements to be placed at the top level of a testbench module to wait until the variable **`clkcnt`** is equal to 5000and then print the string **`Simulation Complete`** and end the simulation.

Write only the statements required to accomplish this, not the complete testbench. You may assume **`clkcnt`** has been declared as **`integer clkcnt`**.

Hint: "top level" means not *inside an* ***`initial`*** *or* ***`always`*** *block.*

Question 4 — 4 marks

The digital circuit below has a 2-bit register with a minimum setup time requirement of 5 ns. The combinational logic path from A to B has a (maximum) delay of 10 ns. The combinational logic path from C to D has a (maximum) delay of 20 ns. The register's clock-to-output delay is 5 ns (maximum). What is the maximum clock *frequency* at which this circuit will operate reliably?



Question 5 — 2 marks

What logic function of the inputs A and B does the following schematic implement? *Briefly* explain your reasoning or show how you obtained your answer. *Hint1: The arrangement of the N- and P-channel MOSFETs is reversed from the NAND and NOR gates in the lecture notes. Hint2: Work out which transistors are on and which are off for all four possible input combinations.*