ELEX 2117 : Digital Techniques 2
2024 Fall Term

MIDTERM EXAM 1
15:30-18:20
Friday, October 4, 2024
SW01-1021

This exam has three (3) questions on four (4) pages. The marks for each question are as indicated. There are a total of seventeen (17) marks. Answer all questions. Write your answers and all rough work in this paper and nowhere else. Show your work. Underline or draw a box around your final answer. Numerical answers must include units. Books and notes are allowed. No electronic devices other than calculators are allowed. **Show your work.**

This exam paper is for:

Sample Exam 1 A00123456

Each exam is equally difficult.

Answer your own exam.

Do not start until you are told.

Name: _____

BCIT ID: _____

Signature: _____

0

Question 1 — 7 marks

Fill the table below with the value of each expression as a Verilog numeric literal including the correct width and the correct value in *hexadecimal* base. Assume the following declarations:

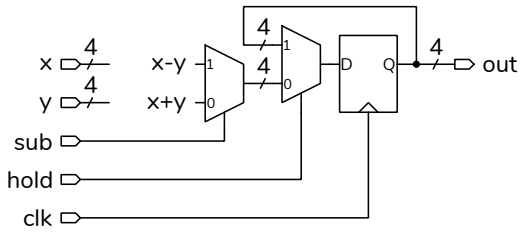
```
logic [7:0] x ;
logic [3:0] y ;
```

and that `x` has the value `8'h5A` and that `y` has the value `4'b0110`. The first row has been filled in as an example. You need not show your work or draw another box around the answer.

expression	value
`x[3:0]`	`4'hA`
`x - y + 4'h4`	
`x[3] ? y : y >> 2`	
`x ? {y,x} : {x,y,x}`	
`x[3:0] ||  x |  y`	
`x != y >= 0`	
`x & y ^ 8'hff`	
`x * y[3:0] && x`	

Question 2 — 5 marks

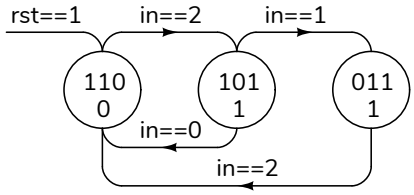
Write a Verilog module named **addsub** that implements the following block diagram. The diagram follows the course conventions for block diagrams. Follow the course coding guidelines but omit comments.



Question 3 — 5 marks

A state machine has a one-bit output named **`out`**, a two-bit input named **`in`**, a one-bit input named **`rst`**, and clock input named **`clock`**.

Write a Verilog module named **`sm2`** that implements the following state transition diagram. The diagram follows the conventions described in the lecture notes. Include all necessary declarations. Follow the course coding guidelines but omit comments.



ELEX 2117 : Digital Techniques 2

2024 Fall Term

MIDTERM EXAM 1

15:30-18:20

Friday, October 4, 2024

SW01-1021

This exam has three (3) questions on four (4) pages. The marks for each question are as indicated. There are a total of seventeen (17) marks. Answer all questions. Write your answers and all rough work in this paper and nowhere else. Show your work. Underline or draw a box around your final answer. Numerical answers must include units. Books and notes are allowed. No electronic devices other than calculators are allowed. **Show your work.**

This exam paper is for:

Sample Exam 2 A01234567

Each exam is equally difficult.

Answer your own exam.

Do not start until you are told.

Name: _____

BCIT ID: _____

Signature: _____

Question 1 — 7 marks

Fill the table below with the value of each expression as a Verilog numeric literal including the correct width and the correct value in *hexadecimal* base. Assume the following declarations:

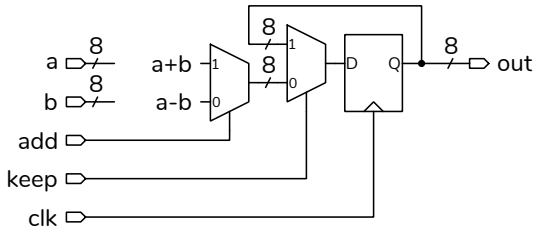
```
logic [7:0] x ;
logic [3:0] y ;
```

and that `x` has the value `8'h83` and that `y` has the value `4'b0110`. The first row has been filled in as an example. You need not show your work or draw another box around the answer.

expression	value
`x[3:0]`	`4'h3`
`x - y + 4'h4`	
`x[3] ? y : y >> 2`	
`x ? {y,x} : {x,y,x}`	
`x[3:0] ||  x |  y`	
`x != y >= 0`	
`x & y ^ 8'hff`	
`x * y[3:0] && x`	

Question 2 — 5 marks

Write a Verilog module named **`alu`** that implements the following block diagram. The diagram follows the course conventions for block diagrams. Follow the course coding guidelines but omit comments.



Question 3 — 5 marks

A state machine has a one-bit output named **`out`**, a two-bit input named **`in`**, a one-bit input named **`rst`**, and clock input named **`clock`**.

Write a Verilog module named **`sm1`** that implements the following state transition diagram. The diagram follows the conventions described in the lecture notes. Include all necessary declarations. Follow the course coding guidelines but omit comments.