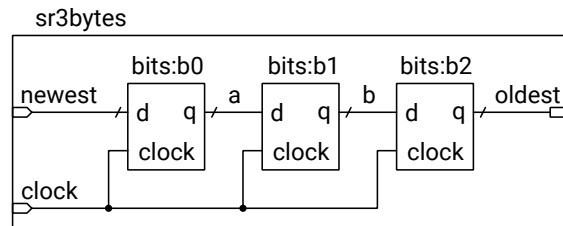


Hierarchical Design

Exercise 1:



Draw a diagram for this instantiation of the `bits` module. Label the module, instance, signal and port names as in the diagram above.

Exercise 2:

```
module sr3bytes
(
    input  logic [7:0] newest,
    output logic [7:0] oldest,
    input  logic clock
) ;

localparam nbits = 8 ;

logic [nbits-1:0] a, b ;

// matching by order
bits #(nbits) b0 (newest,a,clock);

// matching by name (order does not matter)
bits #(.nb(nbits)) b1 (.q(b),.clock,.d(a));

// wildcards for names that match
bits #(.nb(nbits)) b2 (.d(b),.q(oldest),.*);

endmodule
```

Identify the module instantiation statements in the code above. For each one, what is the instantiated module's name? The instance name?