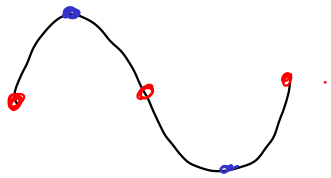
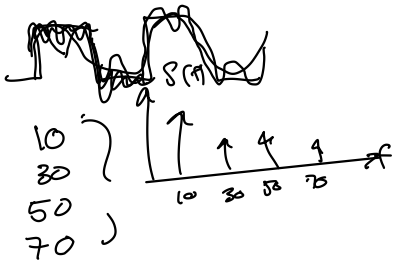
Analog Interfaces

Exercise 1: Draw a sine wave and indicate two sets of sampling points at twice the frequency of the sine wave: one with samples at the zero crossings and one with samples at the peaks of the signal. Is it sufficient to sample at twice the highest frequency of the analog signal?

→ no, need to sample faster.



Exercise 2: What minimum sampling rate would be required to digitize a 10 kHz square wave if you wanted to be able to recover frequency components up to the 7'th harmonic (at 70 kHz)?

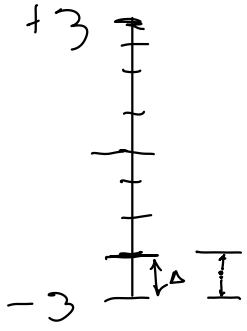


$f_s > 2 \cdot \text{bandwidth}$

$f_s > 2 \cdot 70$

> 140 kHz

Exercise 3: A signal with range of ±3 V must be quantized so that the maximum *quantization error* is less than 1 mV. What is the resolution in mV? What minimum number of bits of resolution is required?



$\Delta = \frac{V}{2^n}$ $\quad 2^n = \frac{V}{\Delta}$

$V = (3-(-3) = 6V$

quantization error $= \frac{\Delta}{2} = 1mV$

$\Delta = 2mV$ — resolution in mV

$n = \log_2 \frac{V}{\Delta}$

$n = \log_2 \frac{6}{.002}$

$= \log_2 3000$

$= 11.55$

use 12 bits

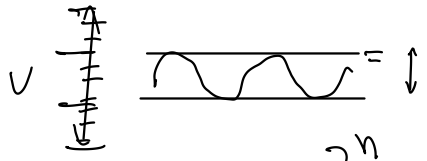
this would give a resolution of $\frac{6}{2^{12}} = 1.46mV$

resolution is 12 bits or 1.46 mV

Exercise 4: When quantizing a full-scale sine wave, what quantization SNR would be achieved with a resolution of 12 bits? What if the signal's voltage range was only half of the full-scale range?

$SNR = 1.76 + 6n$ dB

$= 1.76 + 6 \cdot 12 \approx 73.8$ dB



$SNR = \frac{S}{N}_{(6\text{ dB less})} = 67.8$ dB

now have $\frac{2^n}{2} = 2^{n-1}$ bits of resolution

$20 \log \frac{V_2}{V_1} = 20 \log \frac{1}{2} = -6$ dB

Exercise 5: A signal-to-noise power ratio of about 48 dB is considered "good enough" for speech communication. Assuming the formula above applies for a speech signal, approximately how many bits per sample are required to obtain this quantization SNR? If the speech signal contains frequency components up to 4 kHz, what minimum sampling rate is required? What bit rate is required to store or transmit the digitized signal?

$1.76 + 6n = 48$ dB

$n \approx \frac{48 - 2}{6} = \frac{46}{6} \approx 8$ bits

$f_{sampling} > 2 \times 4$ kHz

> 8 kHz

$8 \frac{\text{bits}}{\text{sample}} \times 8000 \frac{\text{samples}}{\text{sec.}} = \frac{\text{bits}}{\text{sec.}} = 64$ kb/s.

Exercise 6: A DAC outputs a digitized 1 kHz sine-wave signal. The analog output is analyzed and the power at 1 kHz is found to be 1 W while the power at all other frequencies adds up to 10 mW. What is the ENOB?-

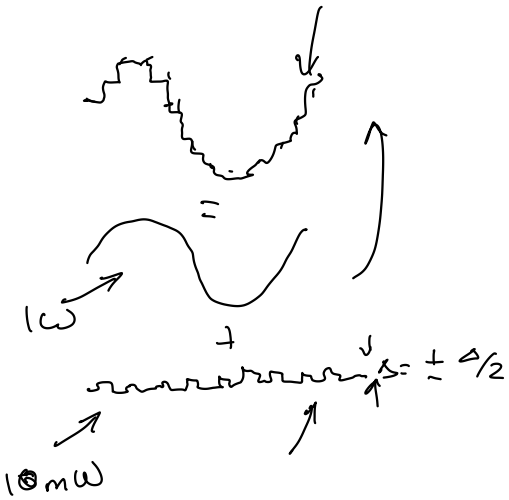
$$SNR = 1.76 + 6n \quad \leftarrow ENOB$$

$$n = \frac{SNR - 1.76}{6}$$

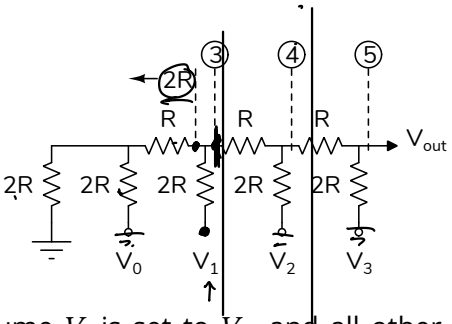
$$SNR = \frac{1}{0.01} = 100 \ W/W$$

$$SNR = 10 \log_{10}(100) = 20 \ dB$$

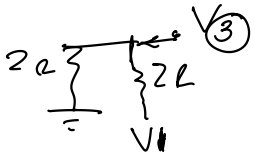
$$ENOB = \frac{20 - 1.76}{6} \approx 3.04$$

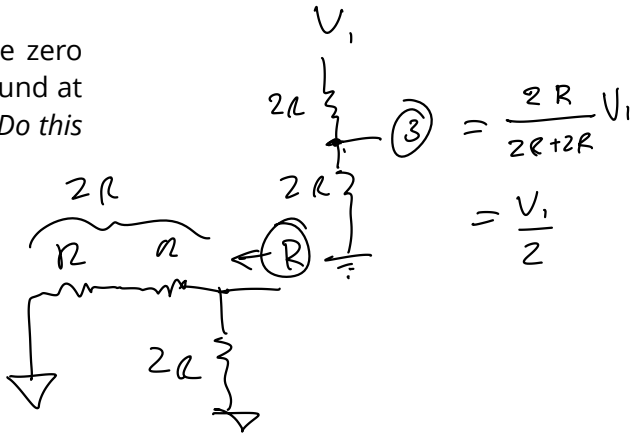


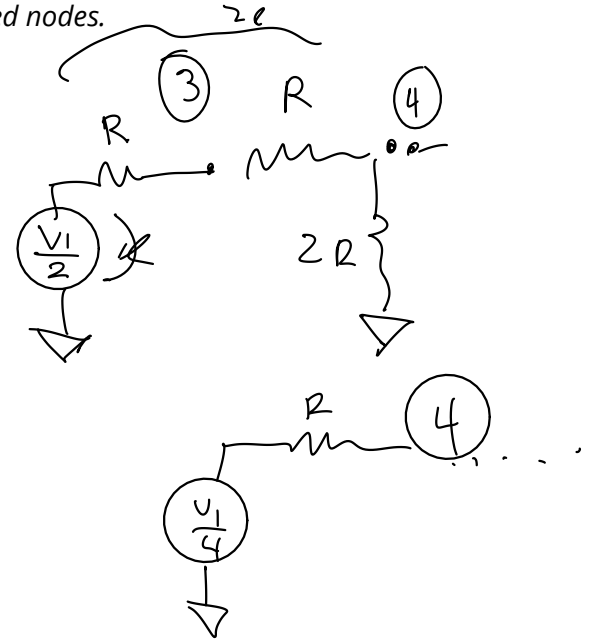
Exercise 7:

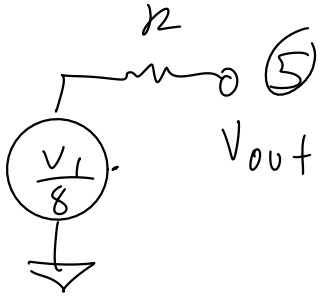


Show this. Assume V_1 is set to V_{ref} and all other inputs are zero (grounded). Find the Thevenim resistance (resistance to ground at V_{out} with all V_i shorted) and voltage (V_{out} with $V_1 = V_{ref}$). *Hint: Do this at the labelled nodes.*

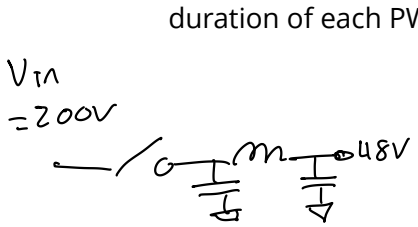


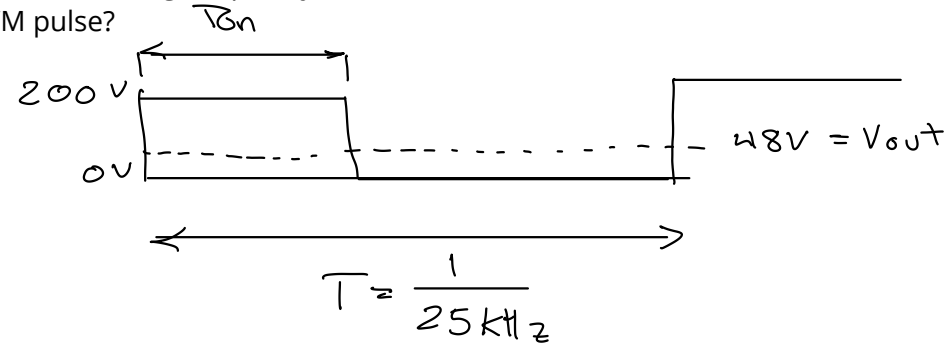






Exercise 8: You are using a PWM DAC to convert a 200 VDC supply to a 48 VDC output. The switching frequency is 25 kHz. What is the duration of each PWM pulse?



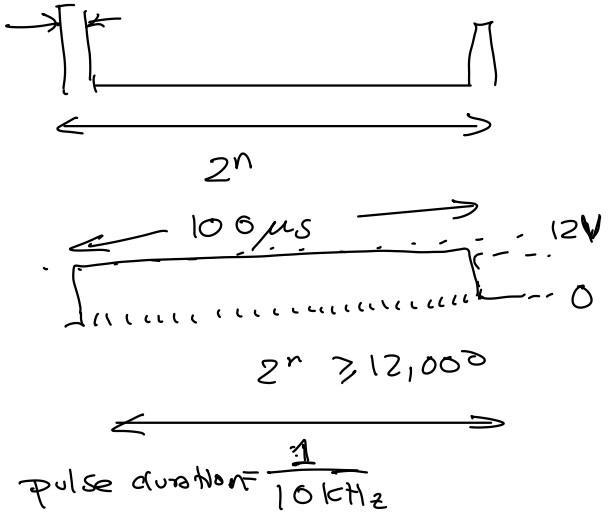


$$\text{duty cycle} = \frac{T_{on}}{T} = \frac{V_{out}}{V_{in}} = \frac{48}{200V}$$

$$T_{on} = T \cdot \frac{48}{200} = \frac{1}{25\times10^3} \cdot \frac{48}{200} = 9.6\,\mu s.$$

Exercise 9: You are designing a PWM DAC and need resolution of 1 mV with a full-scale output of 12 V. How many bits of resolution are required? The pulse frequency is 10 kHz. What is the clock frequency?

resolution = 1mV



$$\frac{12}{1mV} = 12{,}000$$

$2^n \geq 12000$

$n \geq \log_2 12000$

$n \geq 13.5$

use 14 bits $2^n = 16384$

$\therefore f_{clock} = 163{,}840{,}000$

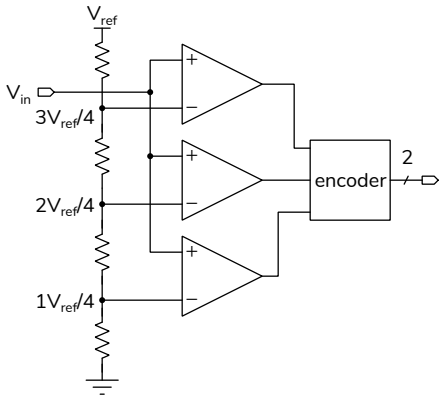
≈ 164 MHz

Exercise 10: Rank the different DACs described above in terms of ~~sampling~~ rate relative to clock rate and complexity relative to resolution.

Pulse

	binary weighted	PWM	Σ-Δ
sampling rate	no clock	$\frac{f_{clock}}{2^n}$	varies.
complexity	2^n resistors	add 1 bit to counter	add 1 bit to n (counter)

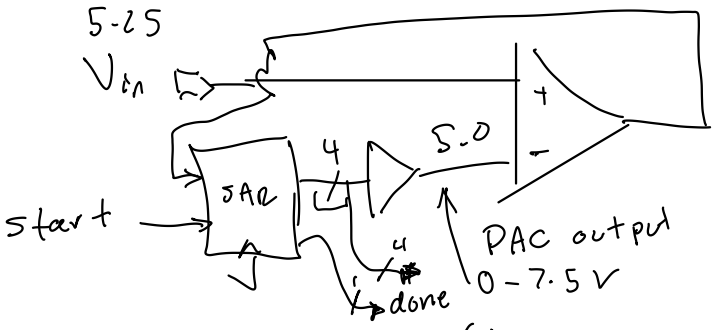
Exercise 11:

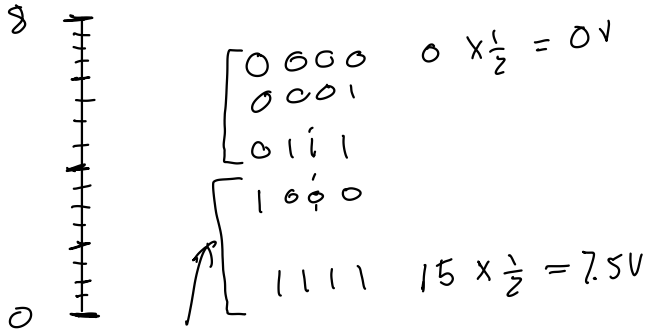


Draw a diagram showing the voltage ranges, the comparator outputs and the binary output for the 4-bit flash ADC above.

comparator outputs	binary output
0 0 0	0 0
0 0 1	0 1
0 1 1	1 0
1 1 1	1 1

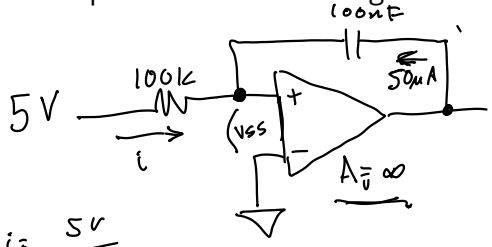
Exercise 12: A SAR ADC using a 4-bit DAC with a full-scale range of 0 to 7.5 V digitizes a 5.25 V signal. What voltages will the DAC output during the conversion?



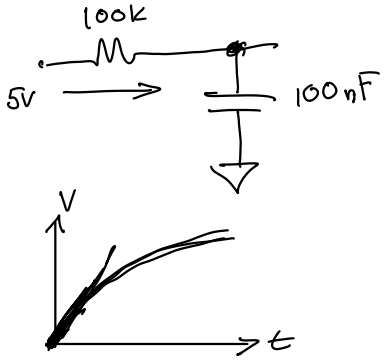


SAR out	DAC out (V)	comparator out (1 = Vin > DAC out)
0 111 (7)	3.5	1
1 011 (11)	5.5	0
1 001 (9)	4.5	1
1 010 (10)	5.0	1
1 011 (11)	5.5	0

Exercise 13: What is the slope of an integrator, in V/s, when charging a 100 nF capacitor with 5 V through a 100 kΩ resistor?



$i = \frac{5V}{100k} = 50\mu A$



$Q = CV$

$i = C\frac{dV}{dt} \longrightarrow \frac{dV}{dt} = \frac{i}{C} = \frac{50\mu A}{100\ nF}$

$i = \frac{dQ}{dt}$

$= \frac{50 \times 10^{-6}}{100 \times 10^{-9}} = 500\ V/s$