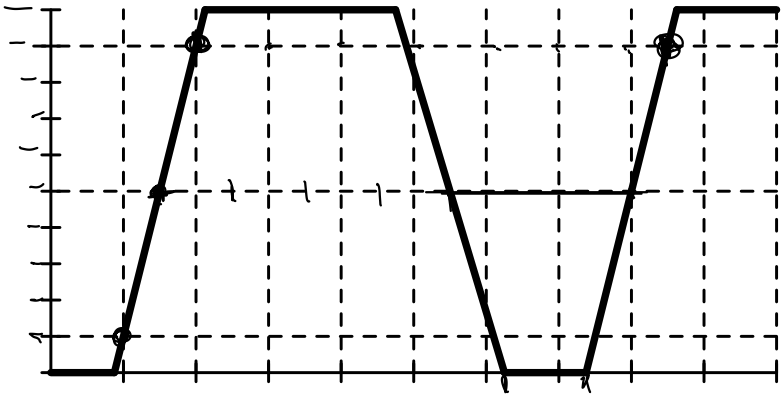
Timing Analysis

Exercise 1:



The diagram above shows an oscilloscope screen capture that includes one period of an *active-low* digital waveform. The scale on the horizontal axis is 20 ns per division. What are: the rise time, period, positive pulse width and duty cycle?

rise time = 1 div. x 20ns/div = 20ns

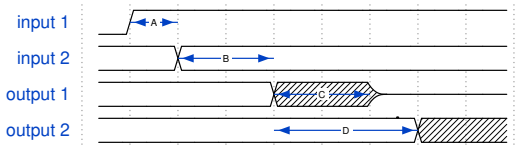
period = 6.5 div x 20ns/div = 130ns.

+ve pulse width = 4 div x 20ns/div = 80ns

-ve pulse " = 2.5 div x 20 = 50ns ← active pulse width

duty cycle = $\frac{50ns}{130ns} = 0.38 = 38\%$

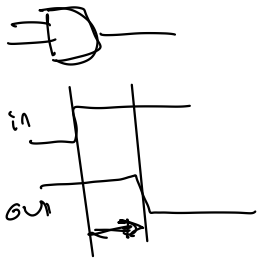
Exercise 2:



Label the specifications A through D as requirements or guaranteed responses. Which specifications are measured to a signal being in a high-impedance state? Which are measured from a rising edge only? From either?

only A ends on an input,
only A is is a requirement.
∴ B, C, D are guaranteed responses
C ends on hi-Z state
A is measured from rising edge
B, C, D are measured from either edge (transition).

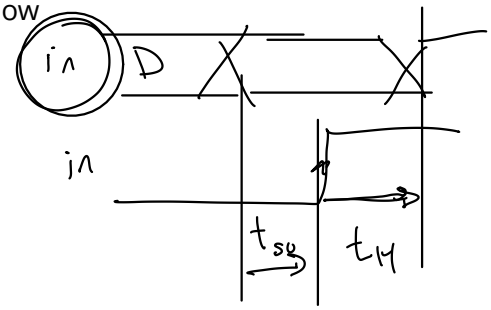
Exercise 3: Is t_{PD} a requirement or a guaranteed response?



Exercise 4: Is t_{SU} a requirement or a guaranteed response? How about t_H?

t_{SU} is a requirement

t_H is a requirement.



Exercise 5:

increases t_{SU} ↑ decrease t_{SU}

t_{SU} (avail) = T_{clock} - t_{CO} (max) - t_{PD} (max)

Which of the specifications in the formula above decrease the available setup time as they increase? Which increase it?

Exercise 6: For a particular circuit f_{clock} is 50 MHz, t_{CO} is 2 ns (maximum), the worst-case (maximum) t_{PD} in a circuit is 15 ns and the minimum setup time requirement is 5 ns. What is the setup time slack? Will this circuit operate reliably? If not, what it the maximum clock frequency at which it will?

$$T_{clock} = \frac{1}{f_{clock}} = \frac{1}{50 \times 10^6} = 20\,ns$$

$$slack = t_{su}(avail) - t_{su}(required) = 3\,ns - 5\,ns = -2\,ns \Rightarrow \text{won't operate reliably.}$$

$$t_{su}(avail) = T_{clock} - t_{CO}^{(max)} - t_{PD}^{(max)} = 20\,ns - 2\,ns - 15\,ns = 3\,ns.$$

at maximum clock frequency slack = 0

$$t_{su}(avail) = t_{su}(rqd) = 5\,ns.$$

$$5\,ns = T_{clock} - 2\,ns - 15\,ns$$

$$T_{clock(max)} = 5 + 2 + 15 = 22\,ns$$

$$f_{clock(max)} = \frac{1}{22\,ns} \approx 45.5\,MHz.$$

Exercise 7: What is the maximum clock frequency for a counter using flip-flops with 200 ps setup times, 50 ps clock-to-output delays and adder logic that has a 250 ps propagation delay?

for f_{max} $t_{su}(avail) = t_{su}(rqd)$

$$t_{su} = T_{clock} - t_{CO} - t_{PD}$$

$$T_{clock} = t_{su} + t_{CO} + t_D = 200 + 50 + 250\,ps = 500\,ps$$

$n = 10^{-9}$
$p = 10^{-12}$

$$f_{clock(max)} = 2\,GHz$$