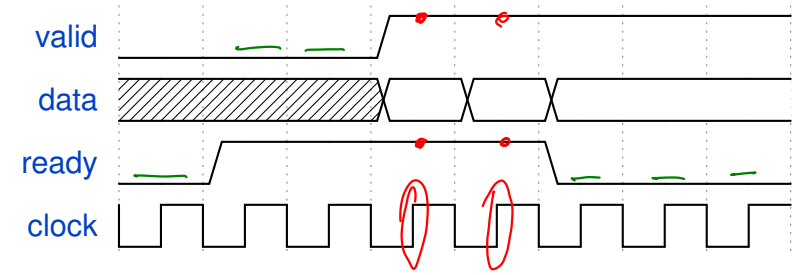
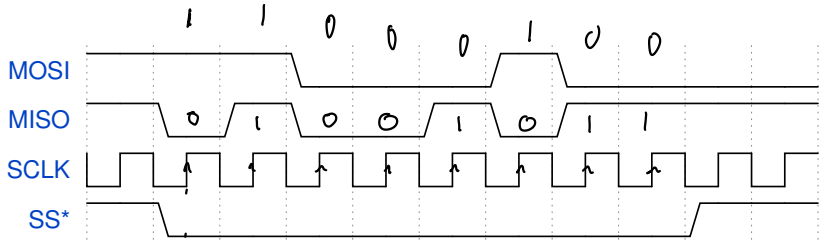
Interfaces

Exercise 1:



Mark the clock edges where data is transferred.

Exercise 2:



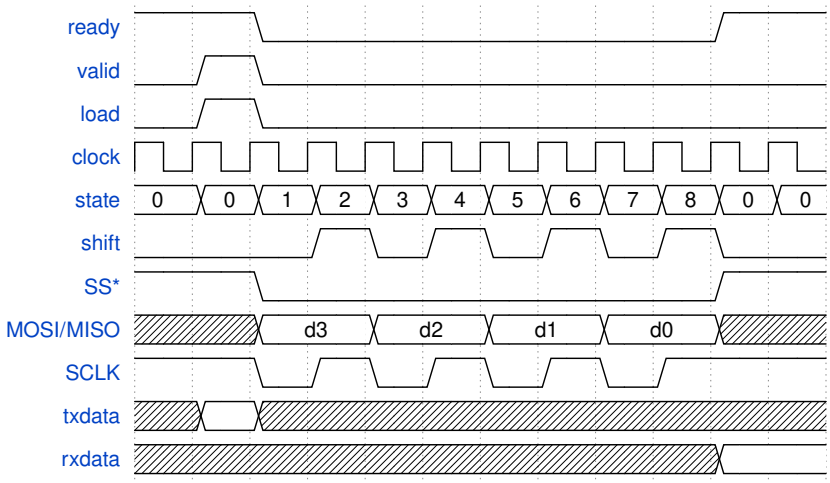
The diagram above shows a transfer over an SPI bus. How many bits of data are transferred? What is the value, in decimal, of the data transferred from the master to the slave? From the slave to the master?

8 bits transferred

on MOSI 196_{10} was Xfered (master to slave).

on MISO 75_{10} " " (slave to master)

Exercise 3:



Based on the diagram above, write a state transition table for an SPI interface controller that transfers four bits at a time. Include an idle state. In which states are **SCLK** and $\overline{\textbf{SS}}$ asserted?

State	input: reset	input: valid	next state
X	1	X	0
0 (idle)	0	1	1
8	0	X	0
n	0	X	n+1