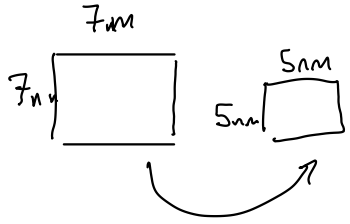
Implementation Technologies

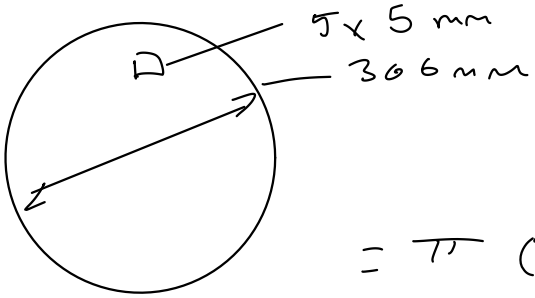
Exercise 1: What improvement in number of transistors per unit area would be achieved by reducing the feature size from 7 nm to 5 nm? Approximately how many 5x5 mm die fit on a 300 mm wafer? How many 200x200 nm gates fit on the die?



$\frac{A}{5^2}$

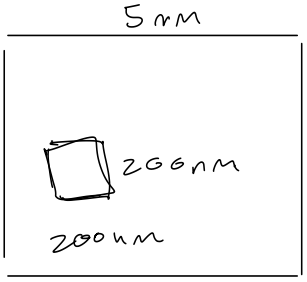
$\frac{A}{7^2}$

ratio of # of die $= \frac{7^2}{5^2} = \frac{49}{25} \approx 2X$



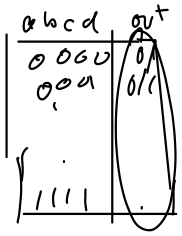
$\frac{\pi r^2}{25} = \frac{\pi (150)^2}{25}$

$= \frac{\pi (30)^2 25}{25} = 2800$



$\left(\frac{5 \times 10^{-3}}{200 \times 10^{-9}}\right)^2 = 625 \times 10^6$

Exercise 2: How many bits are required to program the MAX-V LUT? How many additional bits are required to program the 7 two-input multiplexers that configure the LUT?



16 bits for LUT

7 bits for 7 muxes.

total of 23 bits

Exercise 3: Would you use a PLD or ASIC for: A project that had to be completed within a month? That would be expected to sell 100 million units? Whose complete requirements aren't known? A state-of-the-art general-purpose CPU?

- short TTM – PLD
- high volume – ASIC
- high risk – PLD
- high perf. – ASIC.