Timers and Clock Dividers

You may not submit a video demonstration for this lab. You must demonstrate your solution in person during your scheduled lab session. The lab instructor will then ask you to make changes to demonstrate that you understand your design. You are unlikely to complete this lab unless you start with a working solution.

Introduction

Counters can be used to create delays and periodic signals (clock dividers).

In this lab you will design a circuit that uses two counters to generate a tone of a specific duration and frequency by switching the voltage applied to a speaker on and off.

Your counters will use the 50 MHz clock on the CPLD board. The period of this clock is $T = 1/50\times10^6 = 20$ ns.

Components

You will need:

- your CPLD board, Byte Blaster JTAG interface and mini-USB power connector,
- the matrix keypad
- the speaker from your ELEX 2117 parts kit
- jumpers (or cables with alligator clips on both ends from your ELEX 1117 parts kit[1])

Requirements

The last three digits of your BCIT ID (n_1, n_2, and n_3) determine the key that starts the tone, the tone duration and its frequency.

For example, if your BCIT ID is . A00123 4 5 6 then $n_1 = \boxed{4}$, $n_2 = \boxed{5}$ and $n_3 = \boxed{6}$.

Design your circuit so that:

1. keypad key $\boxed{n_1}$ starts the tone,
2. the frequency of the tone is $f = 500 + n_2 \times 100$ Hz,
3. the tone lasts for $1 + n_3/3$ seconds.

[1] You can put alligator clips over the banana plugs.

For example, for an ID ending in 456, pressing keypad $\boxed{4}$ should generate a $500 + \boxed{5} \times 100 = 1000$ Hz tone for $1 + \boxed{6}/3 = 3$ seconds.

The tone should last for the required duration even if the key is released before the end of the tone duration.

Hints

You can design this circuit using a timer and a clock divider:

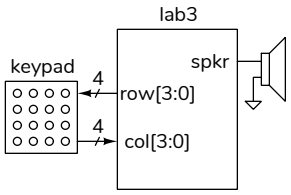
- The timer is a counter that counts from $M - 1$ down to zero each time the appropriate key is pressed. The counter is set to $M - 1$ when the appropriate key is pressed AND the count value is zero. Otherwise, if the counter is not zero, it is decremented by 1. Otherwise the count is unchanged (left at 0). The duration of the timer will be MT where T is the clock period.

- The clock divider is a counter that continuously counts from $N - 1$ down to 0. The clock divider's counter is reset to $N-1$ when the counter reaches zero, otherwise it is decremented by 1. The period of this counter will thus be NT where T is the clock period.

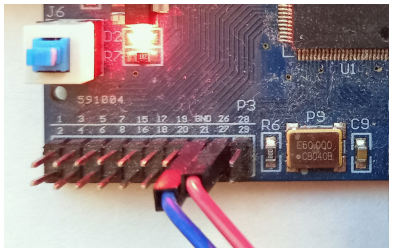
If you set the speaker output high when the timer's counter value is non-zero and the clock divider's counter value is greater than $N/2$ then the speaker output value will be a square wave of the appropriate period and duration.

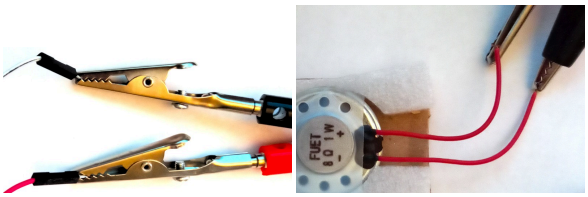
CPLD I/O

The following diagram shows the connections to the CPLD:



Connect the matrix keypad to the CPLD as in previous labs. Connect a CPLD I/O pin to the speaker pin and a ground pin with alligator clip cables (pin 26 was used as the **spkr** pin here, a ground pin is next to it):





Procedure

Create a project, compile it, and configure the CPLD.

If you use the same keypad pins as in the previous lab and Pin 26 for the speaker output, you should end up with the following pin assignments:

To	Assignment Name	Value
row[3]	Location	PIN_99
row[2]	Location	PIN_97
row[1]	Location	PIN_95
row[0]	Location	PIN_91
col[3]	Location	PIN_89
col[2]	Location	PIN_87
col[1]	Location	PIN_85
col[0]	Location	PIN_83
clk50	Location	PIN_12
spkr	Location	PIN_26
led	Location	PIN_77
col	Weak Pull-Up Resistor	On

You can import these pin assignments above from the **lab3.qsf** file on the course website.

For troubleshooting you can assign internal signals to the **led** output on pin 77 . A high level turns on this on-board LED. You can also view this signal with an oscilloscope.

Test your design.

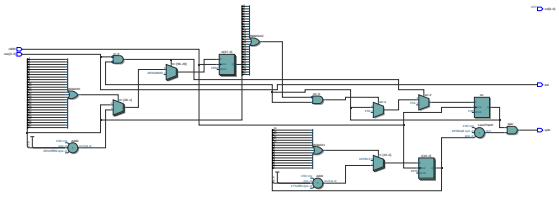
Demonstration and Submission

To get credit for completing this lab you must demonstrate it to the lab instructor during your assigned lab session *and* submit a PDF document containing the following to the appropriate Assignment folder on the course website:

1. (a) The values of n_1, n_2, and n_3 corresponding to your BCIT ID.
   (b) The corresponding button to be pushed, tone frequency and duration.
   (c) The value of **row** for your value of n_1.
   (d) The values of N and M for your values of n_2, and n_3.
   (e) A block diagram of your solution. Follow the instructions in the report and video guidelines document.
2. A listing of your Verilog code.
3. A screen capture of your compilation report (**Window > Compilation Report**) similar to:

Flow Summary	
<<Filter>>	
Flow Status	Successful - Sun Jan 28 18:12:30 2024
Quartus Prime Version	23.1std.0 Build 991 11/28/2023 SC Lite Edition
Revision Name	lab3
Top-level Entity Name	lab3
Family	MAX II
Device	EPM240T100C5
Timing Models	Final
Total logic elements	100 / 240 (42 %)
Total pins	11 / 80 (14 %)
Total virtual pins	0
UFM blocks	0 / 1 (0 %)

4. The schematic created by **Tools > Netlist Viewers > RTL Viewer** and then **File > Export...**. For example:



5. A screen capture of the 'scope measurement of the **spkr** waveform, including a frequency measurement.