Sequential Logic Design with Verilog

Revision 2: Corrected syntax of clock divider instantiation.

Introduction

In this lab you will display the last four digits of your BCIT ID on the 4-digit 7-segment LED display.

You will use the same components as in the previous lab, connected the same way.

Multiplexed LED Display

As shown in the schematic of the LED display in the previous lab, the four digits on the LED display share the same segment (anode) connections. The seven segments on each digit have a common cathode connection. You can therefore only display one digit at a time.

Requirements

Each digit should be displayed, in the correct digit position, for one second. The digits should be displayed in order of increasing value, and repeat.

For example, if your BCIT ID were **A0012 6354** the display should show the following: 3, 4, 5, 6, and then repeat starting with 3.

The display should go blank if 1 is not pressed. Pressing 1 should [re]start from the first digit.

As another example, if your BCIT ID were **A0012 1882** the display should show the following: 1, 2, 8, 8, and then repeat.

Design

One possible solution is described below. It consists of two parts.

One part is a register whose output, **en**, enables the digits one after the other. For example, if you have a clock signal **clk** (see the *Clock* section below):

```
output logic [3:0] en,    // active-low digit enable
 ...
always_ff @(posedge clk)
   en <= ... ;      // next value of en (depends
                    // on values of col and en)
```

The value assigned to **en** in the **always_ff** statement would depend on whether 1 was pressed and on the current value of **en**.

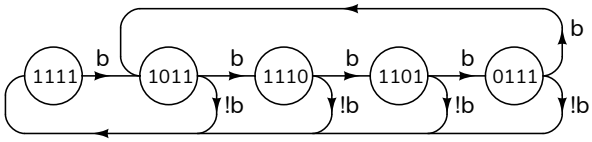
Consider the first example above. The value of **en** should be set to **4'b1111** (all digits off) if 1 is not pressed. If 1 is pressed and **en** is **4'b1111** then **en** should be set to **4'b1011**; if 1 is pressed and **en** is **4'b1011** then it should be set to **4'b1110**; etc. This results in **en** cycling through the four values while 1 is pressed.

Note that the value of **en** only changes on the rising edge (**posedge**) of **clk**.

We can describe this behaviour with a "state transition table":

en	col	next en
any	!= 4'b0111	4'b1111
4'b1111	== 4'b0111	4'b1011
4'b1011	== 4'b0111	4'b1110
4'b1101	== 4'b0111	4'b1101
4'b1110	== 4'b0111	4'b0111

or a "state transition diagram:"



b: col == 4`b0111

where the values in the circles show the values of the register **en**. The arrows labelled b show how **en** changes when 1 is pressed and the arrows labelled !b show how **en** changes when 1 is not pressed.

This means **en** is set to **4'b1111**, regardless of its current value, whenever **b** is false (**col!=4'b0111**). Otherwise the **en**able output cycles through the four other values.

A second part of your design should set the seven segments (**a** through **g**) to the correct values for the digit selected by **en**. This part will be similar to the previous lab.

Component Connections

The CPLD board, keypad and LED display should be connected as in the previous lab. Note that you will need to connect all four digit enables.

Procedure

Follow the Logic Synthesis procedure in the "Software Installation and Use" document along with the changes described below.

Importing Pin Assignments

You can import the pin assignments from the previous lab if you are not changing them – this is recommended. Select **Assignments** / **Import Assignments...** and select **`lab1.qsf`** from your previous lab's project folder as the file. Click on **Categories...**, un-check everything except **Pin and Location Assignments** and click on **OK**. Check that the pin assignments are correct. You may need to add **`en[3]`** through **`en[1]`** which were not used the previous lab. Also check the weak pull-up resistor assignment on the **`col`** inputs which may not have been imported with the pin numbers.

Clock

The board has a 50 MHz clock signal connected to pin 12 of the CPLD. This signal was not used in the previous lab although it was listed in the sample pin assignments and named **`clk50`**. Add this pin assignment if you don't have it already.

You will need to use a supplied "clock divider" module to create a 1 Hz clock from the 50 MHz clock. To do this, copy the **`clkdiv.sv`** file from the course website to your project folder and add it to your project (**Project > Add/remove Files in Project..**). This module has one input, the 50 MHz clock and one output, a clock signal with a configurable frequency. You can instantiate a 1 Hz clock in your **`lab2.sv`** file with the following two lines:

```
logic clk ;
clkdiv #(1) c0 ( clk50, clk ) ;
```

You can then use the **`clk`** signal in your register descriptions:

```
always_ff @(posedge clk) en <= ...
```

Lab Report

Submit the following to the appropriate Assignment folder on the course website:

1. A PDF document containing:
   - A listing of your Verilog code.
   - A screen capture of your compilation report.
   - A block diagram of your design. It should include the inputs and outputs, the clock divider, a state register, and the combinational logic driving the segment outputs.

     Use blocks for: the clock divider instantiation, the combination logic that computes the next **`en`** value, and the combinational logic that computes the segment values – you don't need to include the internal details. Follow the other requirements for block diagrams in the Report and Video Guidelines.
   - a photo of the display when you change the parameter of the **`clkdiv`** module instantiation from 1 to 5000: **`clkdiv #(5000) c0 (clk50, clk ) ;`** and press [1]. The digits in the photo should be upright. For example:

2. If you were not able to demonstrate your solution to the lab instructor during your scheduled lab period, submit a video showing the keypad and the LED display as you: push and hold [1] while your display sequences through at least 5 digits, push [2], push [5], and then push and hold [1] while the display sequences through at least two digits. A sample video demonstration is available on the course website.

Follow the *Report and Video Guidelines* and the *Coding Guidelines* documents on the course website.