Combinational Logic Design with Verilog

Introduction

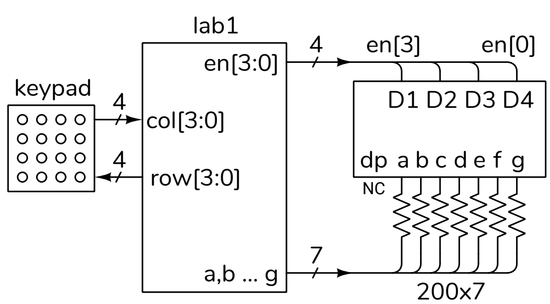
You lab should display one digit at a time on a four-digit 7-segment LED display. Pressing a key on a keypad will select the digit to be displayed.

You will need the components used in the previous lab (CPLD board and USB-Blaster) plus the following:

- solderless breadboard (from previous course)
- 11 M-F ("Dupont" or "Berg") pin-header jumpers (from previous course)
- 4×4 matrix keypad
- seven (7) 200 Ω resistors
- an FJ5463AH 4-digit, 7-segment common-cathode LED display

Circuit Description

The following diagram shows how the keypad and LED are connected to the CPLD and the recommended signal names:



Your circuit should display one of the rightmost four digits of *your* BCIT ID in the rightmost digit position when keys [1] through [A] are pressed. For example, if your BCIT ID were A00123456 then when [1] is pressed the rightmost LED should display 3, when [2] is pressed the rightmost LED should display 4, etc. Otherwise, nothing should be displayed.

Component Connections

CPLD Board

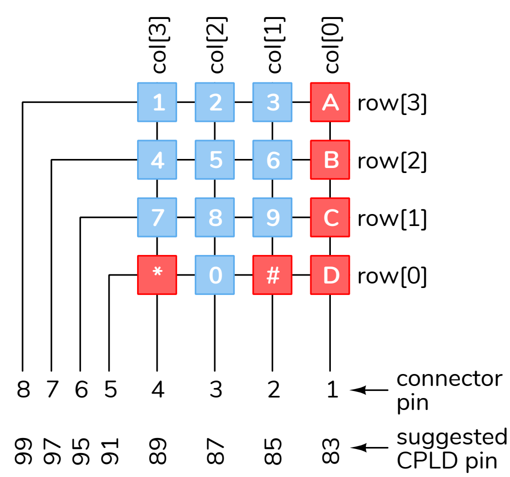
The CPLD has 100 pins. Seventy-six (76) of these are available on four 20-pin headers and will be used to connect components such as the LED display and keypad. The CPLD pin numbers are marked on the PCB. The remaining four header pins provide two grounds, a 3.3 V, and a 5 V supply.

The CPLD's I/O pins use 3.3V logic levels. To avoid damaging the board:

Never connect your circuits to an external power supply or use the on-board 5V supply.

4x4 Matrix Membrane Keypad

The keypad has four horizontal (row) traces and four vertical (column) traces as shown below:

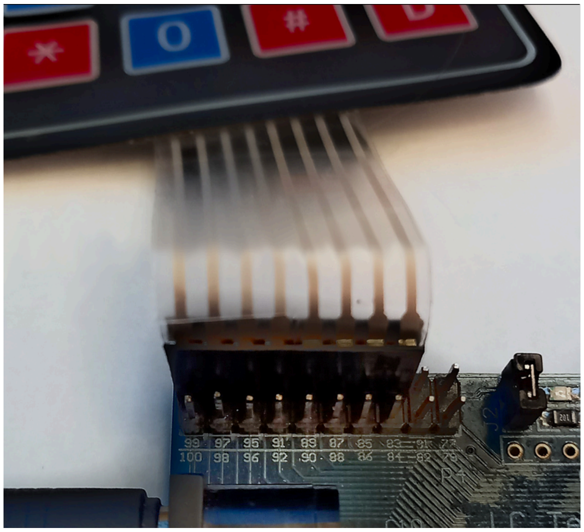


Pressing a key connects a row and column trace. For example, pressing [4] connects `row[2]` to `col[3]`.

The diagram above shows the suggested HDL signal names and the suggested CPLD pin numbers[1].

[1]You may use different pins; for example, if some of your IO pins are damaged.

The keypad connects directly to the top left row of pins if you use the pin numbers above:

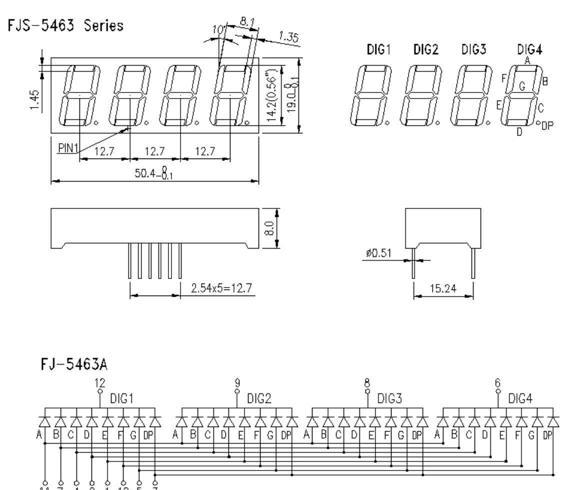


The columns are connected to inputs configured with internal pull-up resistors[2]. Your code must set the top row low and the others high.

Pressing a key along the top row will connect the low logic level to a column input which pulls that column input low. For example, `col` will be `4'b1111` when no key is pushed and `4'b1110` when [A] is pressed. Pushing a key on any other (high) row will have no effect.

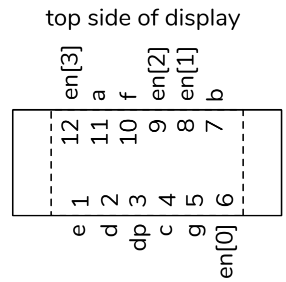
4-digit, 7-segment Multiplexed LED Display

The datasheet for the multiplexed, 4-digit, 7-segment LED display included in your parts kit is shown below:



[2] Using Quartus settings.

The display pinout is:

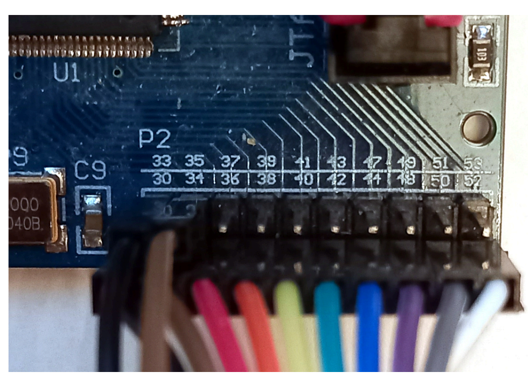


Review the schematic above and notice how the LEDs are connected. This is a multiplexed common-cathode display so you must set the pin for a segment (A-G) high *and* the desired digit enable (DIG1 through DIG4) low to turn on that LED segment on that digit. Only one digit can be displayed at a time because the segment enables are shared by all digits.

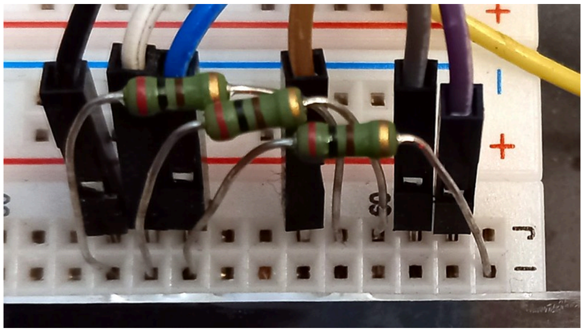
The table below shows one way to connect the CPLD to the display. Note the use of colour coding.

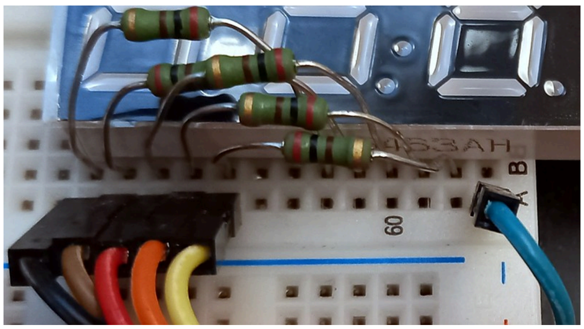
LED Pin	wire colour	seg-ment	CPLD pin
1	black	`e`	30
2	brown	`d`	34
3	red	`dp`	36
4	orange	`c`	38
5	yellow	`g`	40
6	green	`en[0]`	42
7	blue	`b`	44
8	violet	`en[1]`	48
9	gray	`en[2]`	50
10	white	`f`	52
11	black	`a`	33
12	brown	`en[3]`	35

The photo below shows the connections to the CPLD pins:



and the photos below shows the connections to the LED on the breadboard.





The active-low[3] digit-enable outputs are named **en[3]** through **en[0]** from left to right and the active-high segment-enable outputs are **a** through **g** (see the diagram above). Set **en[0]** low and the others high so that only the rightmost digit is enabled.

The segments are connected through 200 Ω resistors to avoid exceeding the CPLD's maximum current specification. The four common cathodes are connected directly.

Procedure

Follow the general procedure in the Software Installation and Use document on the course website to create a project, compile it and configure the CPLD. Connect the CPLD board to the keypad and LED. Test your design and fix any errors.

As an example, the following truth table shows the values of the **col** input, the displayed LED digit and the values of segments a through g for an ID of A00123456:

[3]"Active-low" means an input or output is at a low logic level when it's true. A key would be considered "true" when pressed and an LED segment "true" when lit.

key	col	display	a...g
none	4'b1111		7'b000_0000 (7'h00)
1	4'b0111	3	7'b111_1001 (7'h79)
2	4'b1011	4	7'b011_0011 (7'h33)
3	4'b1101	5	7'b101_1011 (7'h5b)
A	4'b1110	6	7'b101_1111 (7'h5f)

Internal Pull-Up Resistors

When you assign signals to pins you'll also need to configure internal pull-up resistors on the four **col** input pins. Open the Assignment Editor (**Assignments** > **Assignment Editor**). Double-click on «new». in the **To** column and enter the (bus) name (**col**). Select **Weak Pull-Up Resistor** from the drop-down menu in the **Assignment Name** column. Select **On** from the drop-down menu in the **Value** column.

If you used the pin assignments above you should end up with the following[4]:

To	Assignment Name	Value
out a	Location	PIN_33
out b	Location	PIN_44
out c	Location	PIN_38
in clk50	Location	PIN_12
col	Weak Pull-Up Resistor	On
in col[0]	Location	PIN_83
in col[1]	Location	PIN_85
in col[2]	Location	PIN_87
in col[3]	Location	PIN_89
out d	Location	PIN_34
out dp	Location	PIN_36
out e	Location	PIN_30
out en[0]	Location	PIN_42
out en[1]	Location	PIN_48
out en[2]	Location	PIN_50
out en[3]	Location	PIN_35
out f	Location	PIN_52
out g	Location	PIN_40
out row[0]	Location	PIN_91
out row[1]	Location	PIN_95
out row[2]	Location	PIN_97
out row[3]	Location	PIN_99

Hints

1. You can use the Verilog concatenation operator (**{,}**) on the left-hand side of an assignment. For example:

```
...
  assign {a,b,c,d,e,f,g}
    = row == 4'b1011 ? 7'h5b :
...
```

[4]Ignore **clk50** for now, well use it in future labs.

2. To save you time, here are the active-high seven-segment values (`a` to `g`) for digits 0 to 9 in order from most- to least-significant bit[5]:

0	`7'h7e`
1	`7'h30`
2	`7'h6d`
3	`7'h79`
4	`7'h33`
5	`7'h5b`
6	`7'h5f`
7	`7'h70`
8	`7'h7f`
9	`7'h7b`

3. We'll be using the same display in later labs. Leave the LED, resistors and wires connected to your CPLD if you can (if necessary, a small extra breadboard might be worthwhile).

4. You may want to use an AI chatbot such as ChatGPT, Microsoft Copilot, or Perplexity to check your design for errors. They can find errors, explain how the HDL works, suggest improvements, and fix the formatting. Evaluate suggestions carefully – they may not be appropriate for this lab or this course.

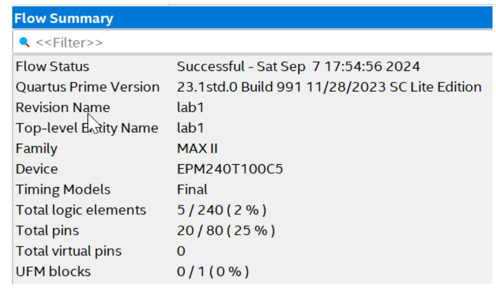
5. You can build and test a bit at a time. For example, you could start by checking that you can detect keypad key presses by using a column input to turn the on-board LED[6] on and off. Then you could check that you can display one digit of your ID.

6. Program your CPLD with the **`lab1.pof`** file on the course website to check your hardware[7].

Lab Report

Submit the following to the appropriate Assignment folder on the course website:

1. A PDF document containing:
   - A block diagram of your design. Label all signals. Use multiplexers for conditional operators and Verilog expressions for other logic. Use Verilog syntax for numeric literals.
   - A listing of your Verilog code.
   - A screen capture of your compilation report, for example:



Flow Summary

<<Filter>>

Flow Status	Successful - Sat Sep 7 17:54:56 2024
Quartus Prime Version	23.1std.0 Build 991 11/28/2023 SC Lite Edition
Revision Name	lab1
Top-level Entity Name	lab1
Family	MAX II
Device	EPM240T100C5
Timing Models	Final
Total logic elements	5 / 240 (2 %)
Total pins	20 / 80 (25 %)
Total virtual pins	0
UFM blocks	0 / 1 (0 %)

2. If you were not able to demonstrate your solution to the lab instructor during your lab period, submit a video showing the breadboard, keypad, and LED display as you push the four keypad keys on the top row from left to right and the keys **5**, **9** and **D**. The rightmost LED should display the last four digits of *your* BCIT ID.

> Follow the *Report and Video Guidelines* and *Coding Guidelines* documents on the course website.

Appendix A - Wire Colour Conventions

Electrons have no fashion sense and so they don't care about the colours of the wires they travel on. However, anyone that needs to follow your wiring will appreciate it if you use a consistent wiring colour scheme, preferably one that they're familiar with.

There's no universal wiring colour scheme, but some conventions are common. For DC circuits: red is the positive supply, black is common, and green is ground. Other colours may mean anything; often these are signals. Be consistent.

Cables with many wires, or wire pairs, often use colour, or colour pairs, to identify circuits rather than to give them meaning.

[5] From Wikipedia.
[6] Connected to pin 77.
[7] Only if you used the same pin assignments as in the lab notes.