ELEX 2117 : Digital Techniques 2
2024 Fall Term

FINAL EXAM
13:00-16:00
Friday, December 13, 2024
SW01-1205

This exam has ten (10) questions on eight (8) pages. The marks for each question are as indicated. There are a total of forty-one (41) marks. Answer all questions. Write your answers and all rough work in this paper and nowhere else. Show your work. Underline or draw a box around your final answer. Numerical answers must include units. Books and notes are allowed. No electronic devices other than calculators are allowed. **Show your work.**

This exam paper is for:

Sample Exam 1 A00123456

Each exam is equally difficult.

Answer your own exam.

Do not start until you are told.

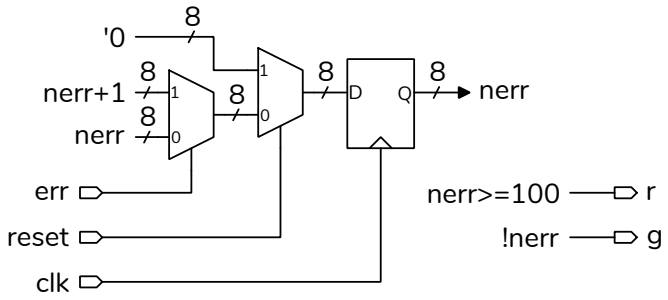
Name: _____

BCIT ID: _____

Signature: _____

Question 1 — 5 marks

The block diagram below follows the course conventions for block diagrams[1]. Write a Verilog module named **`ecnt`** that implements this block diagram, including the module declaration and declarations for signals used within the module. Follow the course coding conventions but omit comments.



[1] Including that the default bus width is 1 bit.

Question 2 — 8 marks

Fill the table below with the value of each expression as a Verilog numeric literal including the correct width and the correct value in *hexadecimal* base. Assume the following declarations:

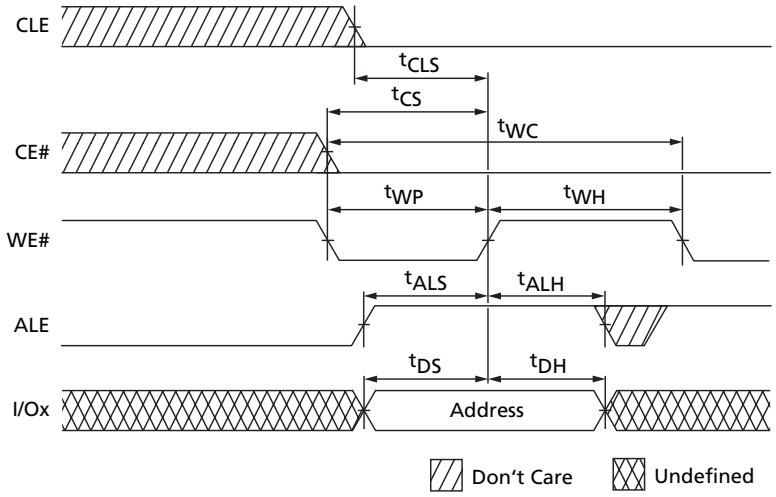
```
logic [7:0] x ;
logic [3:0] y ;
```

and that `x` has the value `8'hA3` and that `y` has the value `4'b0101`. The first row has been filled in as an example. You need not show your work or draw another box around the answer

expression	value
`x[3:0]`	`4'h3`
`x[3:2]`	
`x>>2`	
`{x[7:4], y}`	
`x[1] ? y : y[1:0]`	
`(x && y) + 1`	
`x <= 128 ? x||y : x|y`	
`(3'b100+9'h100)*8'd16`	
`x ^ y & 7`	

Question 3 — 4 marks

The following timing diagram is from the datasheet for the Micron MT29F8G08FABWP NAND flash memory. The suffix **#** indicates an active-low signal (as in **CE#**). All signals shown in the diagram are inputs.



(a) Which timing specifications are "guaranteed responses"?

(b) Which timing specification is a pulse width? *Hint: There is only one.*

(c) Assume **WE#** is a clock signal. (i) Which timing specification(s) is/are setup times? (ii) Which timing specification(s) is/are hold time(s)?

Question 4 — 2 marks

The following specifications are taken from the same IC as in the previous question:

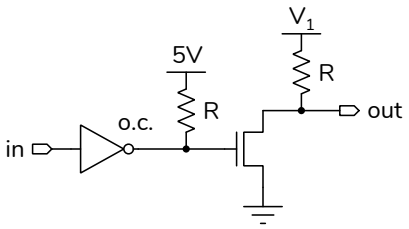
Table 13: DC and Operating Characteristics

Parameter	Conditions	Symbol	Min	Typ	Max	Unit
Input high voltage	I/O [7–0], I/O [15–0] CE#, CLE, ALE, WE#, RE#, WP#, PRE, R/B#	VIH	0.8 x Vcc	–	Vcc + 0.3	V
Input low voltage (all inputs)	–	VIL	-0.3	–	0.8	V
Output high voltage	IOH = -400µA	VOH	0.9 x Vcc	–	–	V
Output low voltage	IOL = 2.1mA	VOL	–	–	0.4	V

Assume V_{cc} is 3.0 V. (a) What is the noise margin for the high logic level? (b) What is the noise margin for the low logic level?

Question 5 — 2 marks

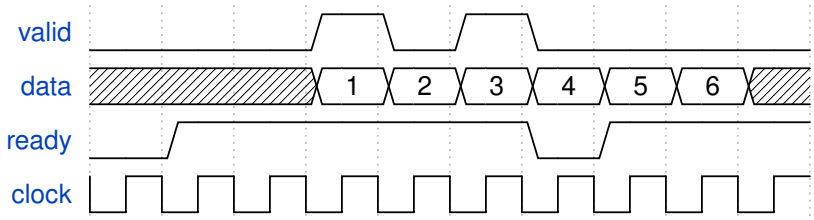
The schematic shows a logic level conversion circuit using an open-collector inverter and an N-channel MOSFET. Assume the on-state resistance of the open-collector output and the MOSFET are much lower than R. V_1 is 20 V.



(a) What is the voltage at **`out`** when **`in`** is at a low logic level? (b) What is the voltage at **`out`** when **`in`** is at a high logic level?

Question 6 — 2 marks

The following timing diagram shows the operation of a ready/valid (FIFO) interface. List the values on the **`data`** line which are transferred over the interface.



Question 7 — 2 marks

The frequency of the **`clk`** signal in the Verilog code below is 5 MHz.

```
logic [11:0] count ;
logic out ;

always_ff @(posedge clk)
   count <= count ? count-1 : 1999 ;

assign out = !count ? 1 : 0 ;
```

Sketch the **`out`** signal (not necessarily to scale) and label the pulse duration and waveform period in microseconds. Show your calculations.

Question 8 — 7 marks

For each term in the left column write the number of the most appropriate match in the right column. There is only one best match for each term. There is no penalty for a wrong answer.

NRE	
Moore's Law	
wafer	
TQFP	
MAX-II	
TSMC	
software	

(1) foundry

(2) package

(3) round

(4) short TTM

(5) mask costs

(6) CPLD

(7) digital ICs

Question 9 — 5 marks

The following Verilog code defines a state machine. The state variable is **`state`**. A one-hot state encoding is used. Draw the state transition diagram. Label the states and state transition conditions using the conventions in lecture notes.

```
module sm
  ( input logic reset, clk,
    input logic [1:0] ab,
    output logic cw ) ;

   logic [2:0] state ;

   always_ff @(posedge clk)
     state <= reset ? 3'b001 :
              state == 3'b001 && ab == 2'b10 ? 3'b010 :
              state == 3'b010 && ab == 2'b01 ? 3'b100 :
              state == 3'b010 && ab == 2'b10 ? 3'b001 :
              state ;
endmodule
```

Question 10 — 4 marks

A module to be tested is declared as:

```
module dut ( input logic clk ; output logic done ) ;
```

Write a Verilog testbench named **`dut_tb`** that instantiates this module, generates a 4 MHz clock signal connected to **`clk`** and terminates the simulation when **`done`** is asserted. Declare all signals used. Your testbench must **not** read or write any files, check for errors, or print any messages.

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Sample Exam 2 A01234567

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Question 1 — 5 marks

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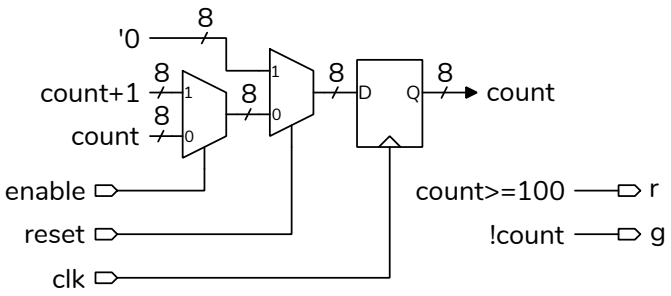

[1] Including that the default bus width is 1 bit.

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```
logic [7:0] x ;
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and that `x` has the value `8'h9c` and that `y` has the value `4'b0101`. The first row has been filled in as an example. You need not show your work or draw another box around the answer

expression	value
`x[3:0]`	`4'hc`
`x[3:2]`	
`x>>2`	
`{x[7:4], y}`	
`x[1] ? y : y[1:0]`	
`(x && y) + 1`	
`x <= 128 ? x||y : x|y`	
`(3'b100+9'h100)*8'd16`	
`x ^ y & 7`	

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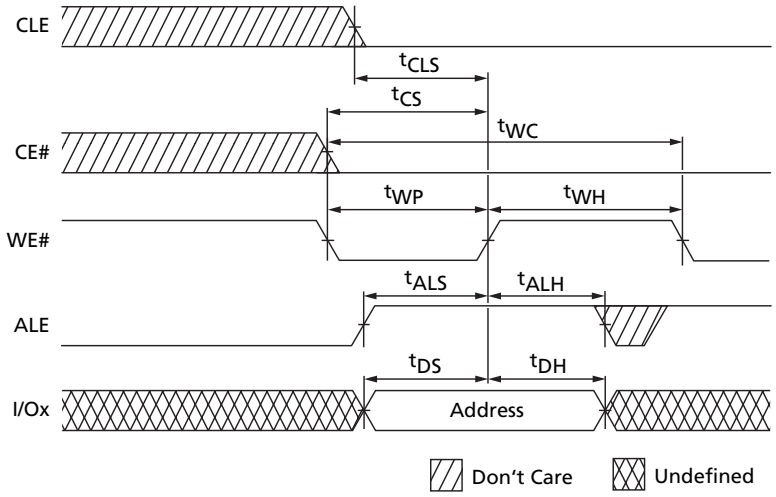

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Assume V_{cc} is 2.7 V. (a) What is the noise margin for the high logic level? (b) What is the noise margin for the low logic level?

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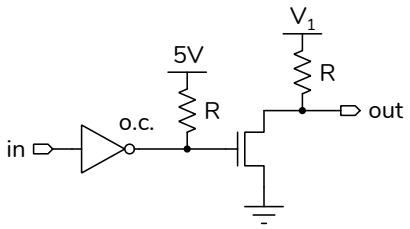
The schematic shows a logic level conversion circuit using an open-collector inverter and an N-channel MOSFET. Assume the on-state resistance of the open-collector output and the MOSFET are much lower than R. V_1 is 10 V.



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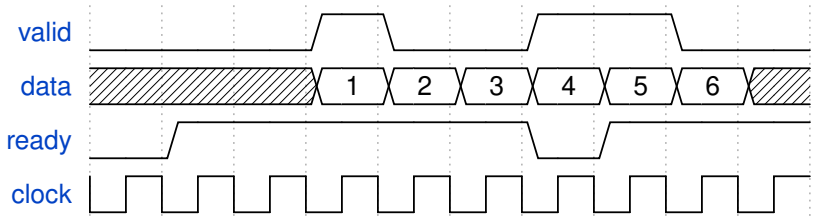

Question 7 — 2 marks

The frequency of the **`clk`** signal in the Verilog code below is 10 MHz.

```
logic [11:0] count ;
logic out ;

always_ff @(posedge clk)
   count <= count ? count-1 : 1999 ;

assign out = !count ? 1 : 0 ;
```

Sketch the **`out`** signal (not necessarily to scale) and label the pulse duration and waveform period in microseconds. Show your calculations.

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              state == 3'b100 && ab == 2'b10 ? 3'b010 :
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endmodule
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