|  |
| --- |
|  |
| ELEX 2117 - Digital Techniques 2 Lab 1: Combinational Logic Design with Verilog  Pre-Lab Report |
| Jane Doe A00123456 |
| September 17, 2021 |

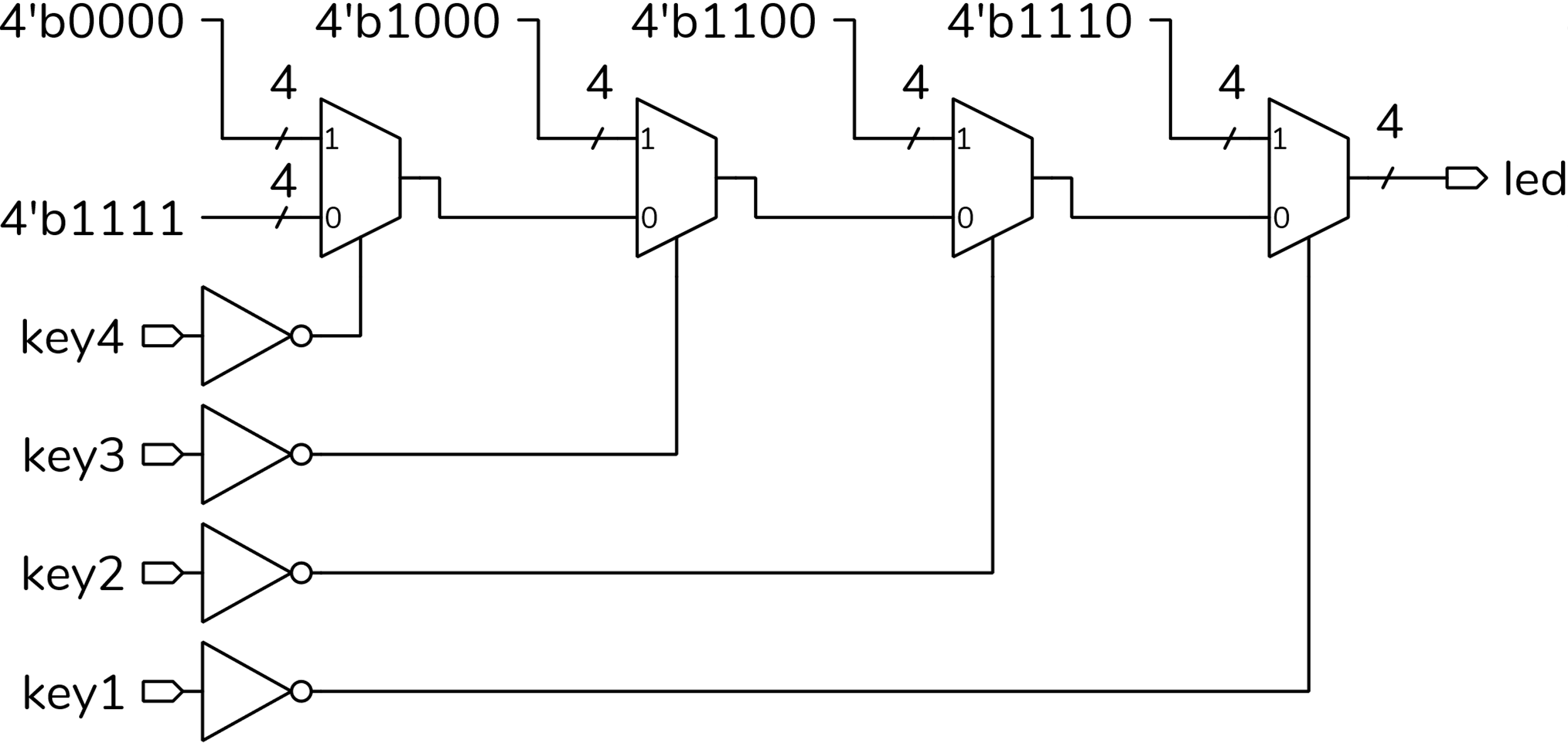
# Instructions

* This template is suitable for ELEX 2117 pre-lab and lab reports.
* Modify the title page as appropriate. Click on the date to update it.
* Apply the ***Heading 1*** style to headings.
* Apply the ***Code*** style to source code. This should apply a monospaced, single-spaced font.
* Use the Snip tool (or equivalent) to copy-and-paste screen captures into your document.
* Exporting (or printing) graphics as PDF usually results in the best quality and smallest file size. Inkscape (and sometimes Word) can open PDF files. You can then select the image and paste it in your report.
* Legible hand-drawn diagrams are acceptable. Crop and rotate appropriately.
* The examples below are typical of what you will need to include in your reports.

# Objectives

|  |  |
| --- | --- |
| Key Pressed | Illuminated LEDs |
| KEY1 | LED1 |
| KEY2 | LED1, LED2 |
| KEY3 | LED1, LED2, LED3 |
| KEY4 | LED1, LED2, LED3, LED4 |

# Block Diagrams





# Source Code

// lab0.sv

// Use pushbuttons to turn on 1 to 4 LEDs.

// Ed. Casas 2021-9-12

module lab0

(

input logic key1, key2, key3, key4,

input logic clk50,

output logic [3:0] led

) ;

// each active-low key selects the appropriate number of active-low

// LEDs

assign led = !key1 ? 4'b1110 :

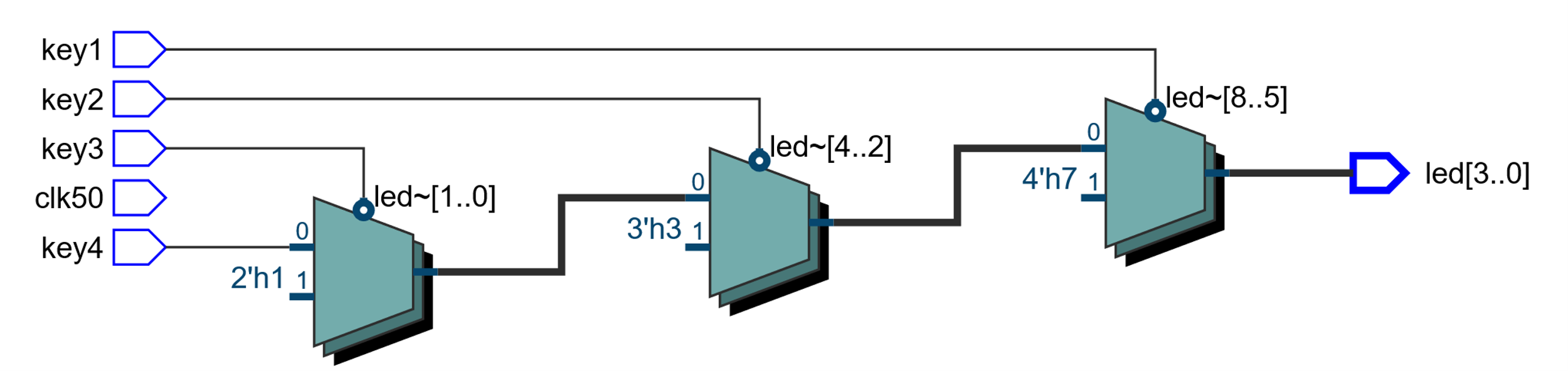
!key2 ? 4'b1100 :

!key3 ? 4'b1000 :

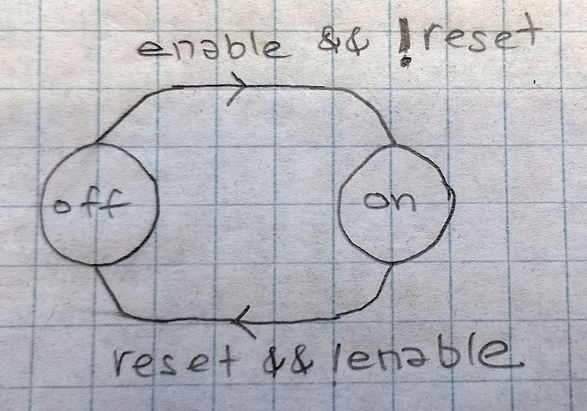
!key4 ? 4'b0000 : 4'b1111 ;

endmodule

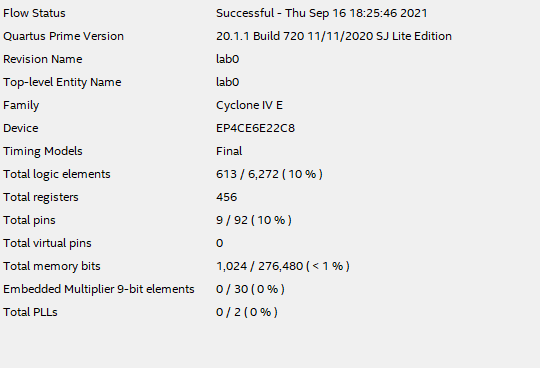
# RTL Netlist



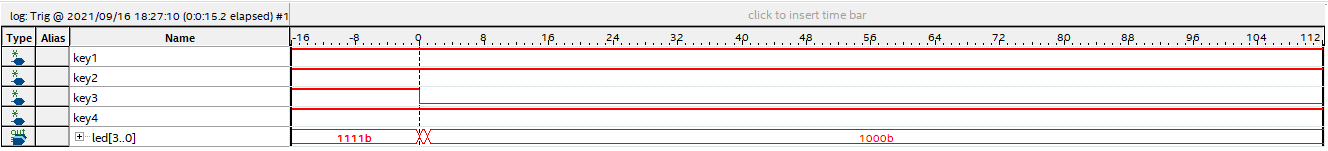
# State Transition Diagram



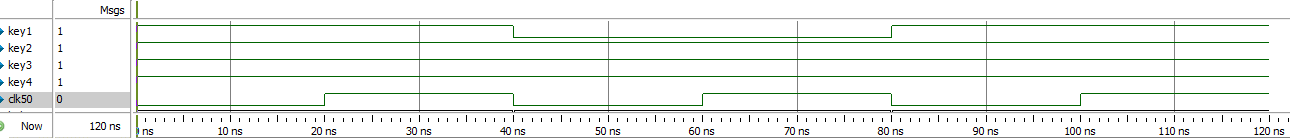
# Compilation Report



# Logic Analyzer Screen Capture



# Simulation Waveforms



# Simulation Transcript

