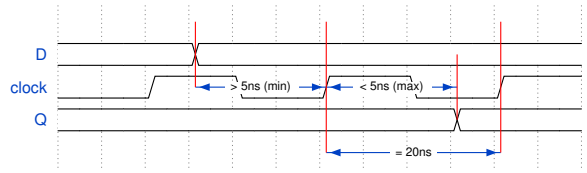
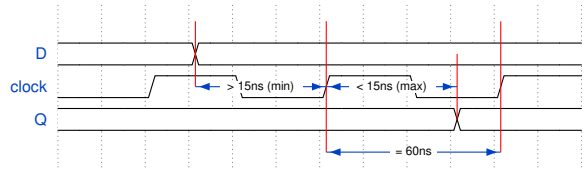
Solutions to Quiz 3

There were two versions of each question. The values and the answers for both versions are given below.

Question 1



or:



The diagram above shows three timing specifications for a register. The signals labelled D, clk, and Q are the register's input, clock, and output respectively. If this register is used in a circuit, what is the maximum propagation delay from Q to D that would result in reliable (non-metastable) behaviour? Show your work.

Answers

The minimum time between a change in D and the rising edge of the clock is the setup time. From the diagram this is $t_{SU} = 5$ ns (or 15 ns),

The maximum time between the rising edge of the clock and valid value on the register output, Q, is the clock-to-output delay. From the diagram this is $t_{CO} = 5$ ns (or 15 ns).

The clock period is the time between any two of the same parts of a periodic waveform. From the diagram this is $T_{clock} = 20$ ns (or 60 ns).

The maximum propagation delay will result in zero slack, which is defined as $t_{SU}(available) - t_{SU}(\text{required})$. Setting this to zero, $t_{SU}(available) = t_{SU}(\text{required})$.

Solving:

$$t_{SU}(\text{avail}) = T_{clock} - t_{CO}(\text{max}) - t_{PD}(\text{max})$$

for $t_{PD}(\text{max})$:

$$t_{PD}(\text{max}) = T_{clock} - t_{CO} - t_{SU}$$

$$= 20 - 5 - 5 = \boxed{10\,\text{ns}}$$

(or $60 - 15 - 15 = \boxed{30\,\text{ns}}$).

Question 2

A digital device consumes 50 mW when operating continuously at 50 MHz. If it operates for half of the time at 50 MHz and half of the time at 10 MHz (or 5 MHz), how much power will it consume on average? Show your work. *Hint: The average of x and y is $(x + y)/2$.*

Answers

Reducing the frequency to 10 MHz reduces power consumption to:

$$\frac{P_2}{P_1} = \frac{f_2}{f_1} \cdot \left(\frac{V_2}{V_1}\right)^2$$

$$\frac{P_2}{50} = \frac{10}{50}$$

So the power at 10 MHz will be 10mW. Since each frequency is used 50% of the time, the average power consumption is $0.5 \times 50 + 0.5 \times 10 = \boxed{30\text{mW}}$.

Similarly, reducing the frequency to 5 MHz reduces the power to 5 mW and the average power consumption to $0.5 \times 50 + 0.5 \times 5 = \boxed{27.5\text{mW}}$.

Question 3

At the output of a DAC you measure the signal power as 100 mW and the noise power as 1.02 µW (or 65.2 µW). What is the SNR in dB? What is the ENOB? Show your work. *Hint: SNR in dB is equal to $10\log_{10}(S/N)$ where S and N are the signal and noise powers (in Watts) respectively.*

Answers

The SNR is $10\log_{10}(^{100\times10^{-3}}/_{1.02\times10^{-6}}) \approx 50\,\text{dB}$. An ENOB of B bits results in a quantization SNR of $\approx 1.76 + 6.02B$. Solving for B, $B \approx (32-2)/6 \approx \boxed{8\text{ bits}}$.

If the SNR is $10\log_{10}(^{100\times10^{-3}}/_{65.2\times10^{-6}}) \approx 32\,\text{dB}$ then $B \approx (50-2)/6 \approx \boxed{5\text{ bits}}$.

Note: Effective number of bits (ENOB) measures a continous variable – noise and distortion – and should not be rounded off to an integer. Marks were not deducted if you did this since this was not explained in the lectures.