ELEX 2117 : Digital Techniques 2
2023 Fall Term

Quiz 2
9:30 – 10:20 PM
Friday, October 20, 2023
SW01-1021

This exam has three (3) questions on two (2) pages. The marks for each question are as indicated. There are a total of nine (9) marks. Answer all questions. Write your answers and all rough work in this paper and nowhere else. Show your work. Underline or draw a box around your final answer. Numerical answers must include units. Books and notes are allowed. No electronic devices other than calculators are allowed. **Show your work.**

This exam paper is for:

Paper, Test 1 A00123456

Each exam is equally difficult.

Answer your own exam.

Do not start until you are told to do so.

Name: _____

BCIT ID: _____

Signature: _____

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Question 1 — 2 marks

(a) A signal named $\overline{\texttt{dry}}$ is at a low logic level. Is it dry (yes or no)?

(b) What logic level would you expect if an alarm signal was indicating a warning and the name of an output was `warning_n` (high or low)?

Question 2 — 2 marks

Fill in the blank boxes in the table below so that all values in each row are consistent (agree with each other). The first row is an example.

signal name	truth value (T/F)	truth value in an expression (0/1)	logic level (H/L)	Verilog value when input (0/1)
$\overline{\texttt{running}}$	T	1	L	0
clear				0
cold*	F			

Question 3 — 5 marks

A module named `m` is declared as:

```
module m
   #(parameter i=4)
   ( input logic [7:0] x, y, c ) ;

endmodule
```

Another module, named `top` is declared as:

```
module top ;

   logic [7:0] a, b, c ;

   assign a = 3 ;
   assign b = 2 ;
   assign c = 1 ;

   m m0 (a,b,c) ;
   m #(2) m1 (.y(b),.x(a),.*) ;
   m #(.i(1)) m2 (a-c,b,a+1) ;

endmodule
```

Fill in the following table with the values of `i`, `x`, `y` and `c` in each instance of the `m` module in the `top` module:

instance	i	x	y	c
m0				
m1				
m2				

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Question 1 — 2 marks

(a) A signal named $\overline{\texttt{wet}}$ is at a high logic level. Is it wet (yes or no)?

(b) What logic level would you expect if an alarm signal was indicating a warning and the name of an output was **`alarm_n`** (high or low)?

Question 2 — 2 marks

Fill in the blank boxes in the table below so that all values in each row are consistent (agree with each other). The first row is an example.

signal name	truth value (T/F)	truth value in an expression (0/1)	logic level (H/L)	Verilog value when input (0/1)
$\overline{\texttt{active}}$	T	1	L	0
smoke*				1
hot	T			

Question 3 — 5 marks

A module named **`m`** is declared as:

```
module m
   #(parameter i=4)
   ( input logic [7:0] x, y, c ) ;

endmodule
```

Another module, named **`top`** is declared as:

```
module top ;

   logic [7:0] a, b, c ;

   assign a = 1 ;
   assign b = 2 ;
   assign c = 3 ;

   m m0 (a,b,c) ;
   m #(1) m1 (.y(b),.x(a),.*) ;
   m #(.i(2)) m2 (c-a,b,a+1) ;

endmodule
```

Fill in the following table with the values of **`i`**, **`x`**, **`y`** and **`c`** in each instance of the **`m`** module in the **`top`** module:

instance	i	x	y	c
m0				
m1				
m2				