

Solutions to Quiz 1

There were two versions of each question. The values and the answers for both versions are given below.

Question 1

Write a Verilog module named `allbits` (or `anybits`) that has one 10-bit logic input named `v` and a (one-bit) logic output named `a`. The value of `a` should be set to the and-(or or-)reduction of `v`.

Answers

```
module allbits
  ( input logic [9:0] v,
    output logic a ) ;

  assign a = &v ;

endmodule
```

```
module anybits
  ( input logic [9:0] v,
    output logic a ) ;

  assign a = |v ;

endmodule
```

Question 2

Write a Verilog literal that has a width of 6 (or 7) bits, uses a hexadecimal (or binary) base and has a value of 12 (decimal).

Answers

6'hc or 7'b1100.

Question 3

Fill the table below with the value of each expression as a Verilog numeric literal including the correct width and the correct value in hexadecimal base. Assume the following declarations:

```
logic [7:0] x ;
logic [3:0] y ;
```

and that `x` has the value 8'h3a (or 8'ha3) and that `y` has the value 4'b1001. The first row has been filled in as an example.

Answers

For `x=8'h3a`:

expression	value
<code>x[3:0]</code>	4'h4
<code>~x[2:0]</code>	3'h5
<code>{ x[7:4], 4'b0011 }</code>	8'h33
<code>^y</code>	1'h0
<code>x[0] ? 1 : 2</code>	32'h2
<code>x >> 2</code>	8'he

and for `x=8'ha3`:

expression	value
<code>x[3:0]</code>	4'h3
<code>~x[2:0]</code>	3'h4
<code>{ x[7:4], 4'b0011 }</code>	8'ha3
<code>^y</code>	1'h0
<code>x[0] ? 1 : 2</code>	32'h1
<code>x >> 2</code>	8'h28

Question 4

Draw a block diagram (a schematic) that corresponds to the following Verilog code:

```
logic [7:0] x, y, z ;
logic a, b ;
assign z = a ? x : b ? y : z ;
```

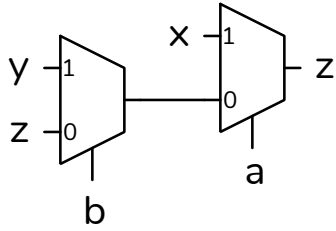
or:

```
logic [7:0] x, y, z ;
logic a, b ;
assign z = a ? ( b ? x : y ) : z ;
```

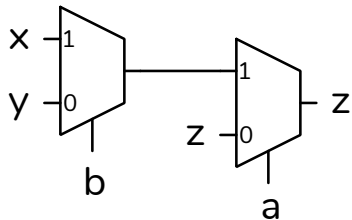
Follow the guidelines in the Diagrams section of the Report and Video Guidelines document.

Answers

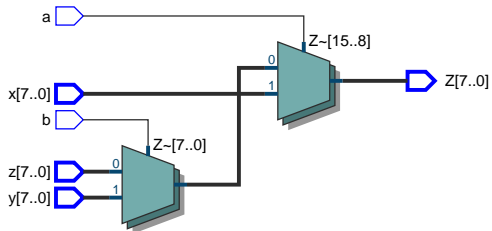
Note: I unintentionally re-used the signal z as both an input and output of a multiplexer. This creates a “latch.” Latches are level-sensitive – rather than edge-sensitive – memory elements. Latches should be avoided and are not commonly used in modern logic design.



or:



Quartus generates the following (using a separate output signal, Z):



and:

