**ELEX 2117 : Digital Techniques 2**
**2023 Fall Term**

**Quiz 1**
**9:30 – 10:20 PM**
**Friday, September 22, 2023**
**SW01-1021**

This exam has four (4) questions on two (2) pages. The marks for each question are as indicated. There are a total of thirteen (13) marks. Answer all questions. Write your answers and all rough work in this paper and nowhere else. Show your work. Draw a box around your final answer. Numerical answers must include units. Books and notes are allowed. No electronic devices other than calculators are allowed. **Show your work.**

This exam paper is for:

# Paper, Test 1 A00123456

Each exam is equally difficult.

Answer your own exam.

Do not start until you are told to do so.

Name: _____

BCIT ID: _____

Signature: _____



0

## Question 1 — 3 marks

Write a Verilog module named **anybits** that has one 10-bit logic input named **v** and a (one-bit) logic output named **a**. The value of **a** should be set to the or-reduction of **v**.

## Question 2 — 2 marks

Write a Verilog literal that has a width of 7 bits, uses a binary base and has a value of 12 (decimal).

## Question 3 — 5 marks

Fill the table below with the value of each expression as a Verilog numeric literal including the correct width and the correct value in hexadecimal base. Assume the following declarations:

```
logic [7:0] x ;
logic [3:0] y ;
```

and that **x** has the value **8'ha3** and that **y** has the value **4'b1001**. The first row has been filled in as an example.

| expression | value |
|---|---|
| x[3:0] | 4'h3 |
| ~x[2:0] | |
| { x[7:4], 4'b0011 } | |
| ^y | |
| x[0] ? 1 : 2 | |
| x >> 2 | |

## Question 4 — 3 marks

Draw a block diagram (a schematic) that corresponds to the following Verilog code:

```
logic [7:0] x, y, z ;
logic a, b ;
assign z = a ? ( b ? x : y ) : z ;
```

Follow the guidelines in the Diagrams section of the Report and Video Guidelines document.

**ELEX 2117 : Digital Techniques 2**

**2023 Fall Term**

**Quiz 1**

**9:30 – 10:20 PM**

**Friday, September 22, 2023**

**SW01-1021**

This exam has four (4) questions on two (2) pages. The marks for each question are as indicated. There are a total of thirteen (13) marks. Answer all questions. Write your answers and all rough work in this paper and nowhere else. Show your work. Draw a box around your final answer. Numerical answers must include units. Books and notes are allowed. No electronic devices other than calculators are allowed. **Show your work.**

This exam paper is for:

# Paper, Test 2 A00123456

Each exam is equally difficult.

Answer your own exam.

Do not start until you are told to do so.

Name: _____

BCIT ID: _____

Signature: _____

## Question 1 — 3 marks

Write a Verilog module named `allbits` that has one 10-bit logic input named `v` and a (one-bit) logic output named `a`. The value of `a` should be set to the and-reduction of `v`.

## Question 2 — 2 marks

Write a Verilog literal that has a width of 6 bits, uses a hexadecimal base and has a value of 12 (decimal).

## Question 3 — 5 marks

Fill the table below with the value of each expression as a Verilog numeric literal including the correct width and the correct value in hexadecimal base. Assume the following declarations:

```
logic [7:0] x ;
logic [3:0] y ;
```

and that `x` has the value `8'h3a` and that `y` has the value `4'b1001`. The first row has been filled in as an example.

| expression | value |
|---|---|
| `x[3:0]` | `4'ha` |
| `~x[2:0]` | |
| `{ x[7:4], 4'b0011 }` | |
| `^y` | |
| `x[0] ? 1 : 2` | |
| `x >> 2` | |

## Question 4 — 3 marks

Draw a block diagram (a schematic) that corresponds to the following Verilog code:

```
logic [7:0] x, y, z ;
logic a, b ;
assign z = a ? x : b ? y : z ;
```

Follow the guidelines in the Diagrams section of the Report and Video Guidelines document.