ELEX 2117 : Digital Techniques 2
2023 Fall Term

MIDTERM EXAM 2
15:30
Friday, November 3, 2023
SW03-1750

This exam has four (4) questions on two (2) pages. The marks for each question are as indicated. There are a total of fourteen (14) marks. Answer all questions. Write your answers and all rough work in this paper and nowhere else. Show your work. Underline or draw a box around your final answer. Numerical answers must include units. Books and notes are allowed. No electronic devices other than calculators are allowed. **Show your work.**

This exam paper is for:

Sample Exam 1 A00123456

Each exam is equally difficult.

Answer your own exam.

Do not start until you are told to do so.

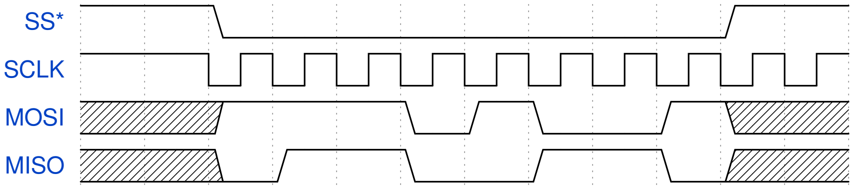
Name: ______________________________

BCIT ID: ______________________________

Signature: ______________________________

Question 1 2 marks

The following waveform shows the signals on an SPI interface. What value was transmitted *from the slave to the master* assuming the bits were transferred most-significant-bit first? Give you answer as a Verilog numeric literal in hexadecimal base, including the width. Show your work.



Question 2 3 marks

For the following testbench:

```
module mt2 ;

   integer n ;
   logic clk ;

   initial begin
      // $dumpfile("ex74b.vcd"); $dumpvars ;
      n = 0 ;
      clk = 0 ;
      wait ( n > 5 ) $stop ;
   end

   always #2us clk = ~clk ;

   always @(posedge clk) begin
      $display("n = %d",n) ;
      n = n + 1 ;
   end

endmodule
```

(a) What is the frequency of the **clk** signal?

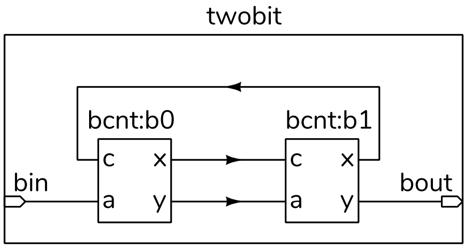
(b) Write the first line that is printed by this testbench:

(c) Write the last line that is printed by this testbench:

Question 3 4 marks

The following Verilog shows the declaration of a module named **bcnt**. The diagram shows how two of these are connected within a module named **twobit**:

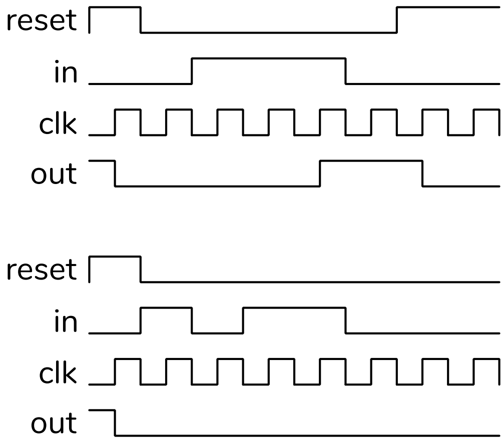
```
module bcnt
( input  logic c, a,
  output logic x, y ) ;
// ...
endmodule
```



The identifiers above the boxes show the module and instance names. The identifiers above the ports show the **twobit** module's port names.

Write a System Verilog module named **twobit** that implements the diagram above. Declare any signal(s) required to implement the **twobit** module. Do not write the **bcnt** module. You may use any style to connect signals to ports. Follow the course coding guidelines but omit comments.

Question 4 5 marks



A state machine has an output named **out** and three inputs named **reset**, **clk**, and **in**.

out changes only on the rising edge of the clock, **clk**. **out** is set to 0 when **reset** is asserted. **out** is set to 1 when **reset** has been low and **in** has been high for 3 consecutive rising edges of the clock. Once **out** is set to 1, it remains set to 1 until **reset** is asserted. Example waveforms are shown.

Fill in the missing code in the following Verilog module so as to implement this state machine. You may use any state encoding. Follow the course coding guidelines but omit comments.

```
module pulsedetect
( input logic reset, clk, in,
  output logic out ) ;

endmodule
```

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This exam paper is for:

Sample Exam 2 A01234567

Each exam is equally difficult.

Answer your own exam.

Do not start until you are told to do so.

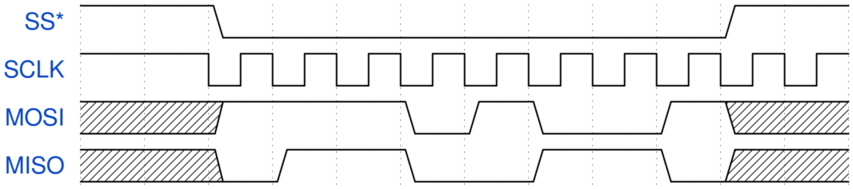
Name: ______________________________

BCIT ID: ______________________________

Signature: ______________________________

Question 1 2 marks

The following waveform shows the signals on an SPI interface. What value was transmitted *from the master to the slave* assuming the bits were transferred most-significant-bit first? Give you answer as a Verilog numeric literal in hexadecimal base, including the width. Show your work.



Question 2 3 marks

For the following testbench:

```
module mt2 ;

   integer n ;
   logic clk ;

   initial begin
      // $dumpfile("ex74a.vcd"); $dumpvars ;
      n = 1 ;
      clk = 0 ;
      wait ( n >= 5 ) $stop ;
   end

   always #4us clk = ~clk ;

   always @(posedge clk) begin
      $display("n = %d",n) ;
      n = n + 1 ;
   end

endmodule
```

(a) What is the frequency of the **clk** signal?

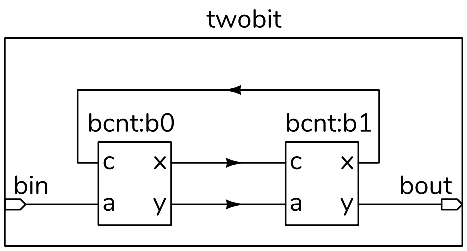
(b) Write the first line that is printed by this testbench:

(c) Write the last line that is printed by this testbench:

Question 3 4 marks

The following Verilog shows the declaration of a module named **bcnt**. The diagram shows how two of these are connected within a module named **twobit**:

```
module bcnt
( input  logic c, a,
  output logic x, y ) ;
// ...
endmodule
```

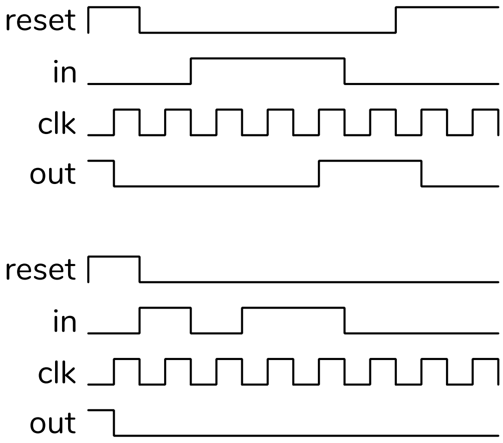


The identifiers above the boxes show the module and instance names. The identifiers above the ports show the **twobit** module's port names.

Write a System Verilog module named **`twobit`** that implements the diagram above. Declare any signal(s) required to implement the **`twobit`** module. Do not write the **`bcnt`** module. You may use any style to connect signals to ports. Follow the course coding guidelines but omit comments.

Question 4 5 marks

A state machine has an output named **`out`** and three inputs named **`reset`**, **`clk`**, and **`in`**.
`out` changes only on the rising edge of the clock, **`clk`**. **`out`** is set to 0 when **`reset`** is asserted. **`out`** is set to 1 when **`reset`** has been low and **`in`** has been high for 3 consecutive rising edges of the clock. Once **`out`** is set to 1, it remains set to 1 until **`reset`** is asserted. Example waveforms are shown.
Fill in the missing code in the following Verilog module so as to implement this state machine. You may use any state encoding. Follow the course coding guidelines but omit comments.



```
module pulsedetect
( input logic reset, clk, in,
  output logic out ) ;

endmodule
```