ELEX 2117 : Digital Techniques 2
2023 Fall Term

MIDTERM EXAM 1
15:30
Friday, October 6, 2023
SW03-1750

This exam has four (4) questions on two (2) pages. The marks for each question are as indicated. There are a total of seventeen (17) marks. Answer all questions. Write your answers and all rough work in this paper and nowhere else. Show your work. Underline or draw a box around your final answer. Numerical answers must include units. Books and notes are allowed. No electronic devices other than calculators are allowed. **Show your work.**

This exam paper is for:

Sample Exam 1 A00123456

Each exam is equally difficult.

Answer your own exam.

Do not start until you are told to do so.

Name: _____

BCIT ID: _____

Signature: _____

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Question 1 — 5 marks

Fill the table below with the value of each expression as a Verilog numeric literal including the correct width and the correct value in hexadecimal base. Assume the following declarations:

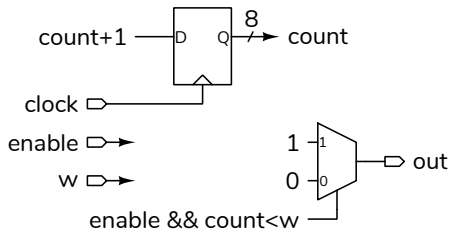
```
logic [7:0] x ;
logic [3:0] y ;
```

and that `x` has the value `8'hb3` and that `y` has the value `4'b0110`. The first row has been filled in as an example.

expression	value
`x[3:0]`	`4'h3`
`!x[4] | x[3]`	
`{ ~y, x[7:4] }`	
`x << y[3:2]`	
`x[7] ? 3'b1 : 4'd2`	
`x + 1`	

Question 2 — 4 marks

Write a System Verilog module named `pwm` with three inputs (`clock`, `enable`, and `w`) and one output (`out`) that implements the schematic below. Follow the course coding conventions.



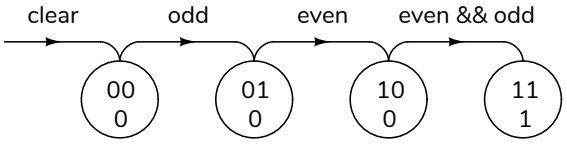
Question 3 — 4 marks

A state machine has `reset` and `clock` inputs, and a `pulse` output. Whenever `reset` is asserted, the output is set to `0`. When `reset` is de-asserted, `pulse` is set to `1` for three clock cycles and then it is set to `0` and it stays at `0` until `reset` is asserted again. Write the next-state truth table and the output truth table for this state machine. Use a binary state encoding.

Question 4 — 4 marks

Write a System Verilog module named **`esc`** that implements the state machine described by the following state transition diagram. The module has four one-bit inputs: **`clear`**, **`even`**, **`odd`**, and **`clock`** (a clock). It has a one-bit output named **`done`**. You may use any name(s) for signal(s) internal to the module.

Follow the course coding conventions.



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This exam paper is for:

Sample Exam 2 A01234567

Each exam is equally difficult.

Answer your own exam.

Do not start until you are told to do so.

Name: _____

BCIT ID: _____

Signature: _____

255

Question 1 — 5 marks

Fill the table below with the value of each expression as a Verilog numeric literal including the correct width and the correct value in hexadecimal base. Assume the following declarations:

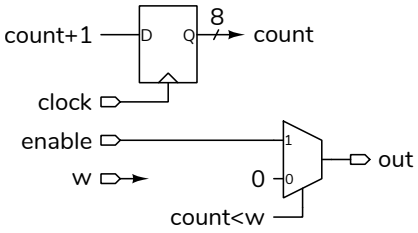
```
logic [7:0] x ;
logic [3:0] y ;
```

and that `x` has the value `8'h3b` and that `y` has the value `4'b0110`. The first row has been filled in as an example.

expression	value
`x[3:0]`	`4'hb`
`!x[4] | x[3]`	
`{ ~y, x[7:4] }`	
`x << y[3:2]`	
`x[7] ? 3'b1 : 4'd2`	
`x + 1`	

Question 2 — 4 marks

Write a System Verilog module named `pwm` with three inputs (`clock`, `enable`, and `w`) and one output (`out`) that implements the schematic below. Follow the course coding conventions.



Question 3 — 4 marks

A state machine has `reset` and `clock` inputs, and a `pulse` output. Whenever `reset` is asserted, the output is set to `0`. When `reset` is de-asserted, `pulse` is set to `1` for three clock cycles and then it is set to `0` and it stays at `0` until `reset` is asserted again. Write the next-state truth table and the output truth table for this state machine. Use a one-hot state encoding.

Question 4 — 4 marks

Write a System Verilog module named **`esc`** that implements the state machine described by the following state transition diagram. The module has four one-bit inputs: **`clear`**, **`even`**, **`odd`**, and **`clock`** (a clock). It has a one-bit output named **`done`**. You may use any name(s) for signal(s) internal to the module.

Follow the course coding conventions.