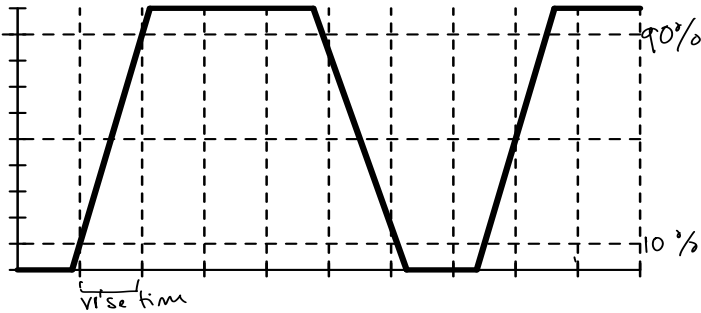


## Timing Analysis

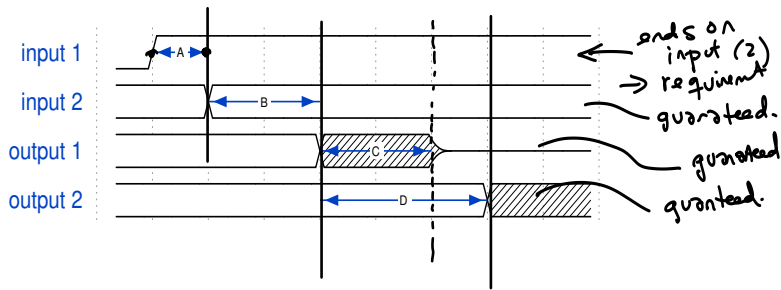
### Exercise 1:



$$\begin{aligned} \text{rise time} &= 1 \text{ div} = 20 \text{ ns} \\ \text{period} &= 6.5 \text{ div} \times 20 \text{ ns/div} = 130 \text{ ns} \\ \text{the pulse width} &= 4 \text{ div} \cdot 20 \text{ ns/div} = 80 \text{ ns} \\ \left( \text{low for } 2.5 \cdot 20 \right) &= \frac{50 \text{ ns}}{130 \text{ ns}} \approx 38.4\% \end{aligned}$$

The diagram above shows an oscilloscope screen capture that includes one period of an *active-low* digital waveform. The scale on the horizontal axis is 20 ns per division. What are: the rise time, period, positive pulse width and duty cycle?

### Exercise 2:



Label the specifications A through D as requirements or guaranteed responses. Which specifications are measured to a signal being in a high-impedance state? Which are measured from a rising edge only? From either?

### Exercise 3: Is $t_{PD}$ a requirement or a guaranteed response?

measured to an output  $\Rightarrow$  guaranteed response

### Exercise 4: Is $t_{SU}$ a requirement or a guaranteed response? How about $t_H$ ?

$t_{SU} \rightarrow$  measured from D to  $\downarrow$  clock  
 $\Rightarrow$  requirement

$t_H \rightarrow$  measured from  $\downarrow$  clock to D  
 $\Rightarrow$  requirement.

**Exercise 5:**

$$t_{su}(\text{avail}) = T_{\text{clock}} - t_{co}(\text{max}) - t_{pd}(\text{max})$$

Which of the specifications in the formula above decrease the available setup time as they increase? Which increase it?

$T_{\text{clock}}$  increases ( $t_{su}$  avail)  
 $T_{co}$  &  $t_{pd}$  decrease  $t_{su}$  (avail)

**Exercise 6:** For a particular circuit  $f_{\text{clock}}$  is 50 MHz,  $t_{co}$  is 2 ns (maximum), the worst-case (maximum)  $t_{pd}$  in a circuit is 15 ns and the minimum setup time requirement is 5 ns. What is the setup time slack? Will this circuit operate reliably? If not, what is the maximum clock frequency at which it will?

$$t_{su}(\text{avail}) = T_{\text{clock}} - t_{co}(\text{max}) - t_{pd}(\text{max})$$

$$\text{slack} = t_{su}(\text{available}) - t_{su}(\text{required})$$

$$T_{\text{clock}} = \frac{1}{50 \times 10^6} = \frac{1000}{50 \times 10^9} = 20 \times 10^{-9} = 20 \text{ ns}$$

$$t_{su}(\text{avail}) = 20 - 2 - 15 = 3 \text{ ns}$$

$$t_{su}(\text{reqd}) = 5 \text{ ns}$$

$$\text{slack} = 3 - 5 = -2 \text{ ns} \quad \begin{array}{l} \text{negative slack} \\ \rightarrow \text{possible metastable} \\ \text{(unreliable) behaviour} \end{array}$$

for  $\text{slack} = 0$  need  $t_{su}(\text{avail}) = 5 \text{ ns}$ .

$$5 = T_{\text{clock}} - 2 - 15$$

$$T_{\text{clock}} = 5 + 2 + 15 = 22 \text{ ns}$$

$$f_{\text{clock}} = \frac{1}{T_{\text{clock}}} = \frac{1}{22 \times 10^{-9}} \approx 45.5 \text{ MHz}$$

**Exercise 7:** What is the maximum clock frequency for a counter using flip-flops with 200 ps setup times, 50 ps clock-to-output delays and adder logic that has a 250 ps propagation delay?

$$t_{su}(\text{reqd}) = 200 \text{ ps}$$

$$t_{co} = 50 \text{ ps}$$

$$t_{pd} = 250 \text{ ps}$$

$$t_{su}(\text{avail}) = t_{su}(\text{reqd}) = 200 = T_{\text{clock}} - t_{co} - t_{pd}$$

$$= T_{\text{clock}} - 50 - 250$$

$$T_{\text{clock}} = 200 + 50 + 250 = 500 \text{ ps}$$

$$f_{\text{clock}} = 2 \text{ GHz}$$