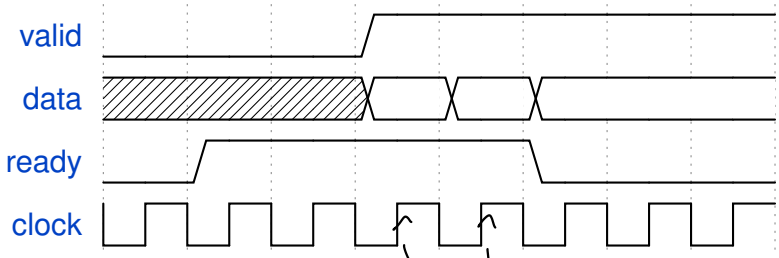
Interfaces

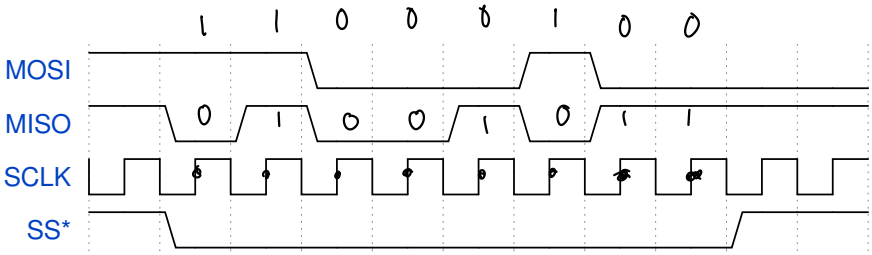
Exercise 1:



Mark the clock edges where data is transferred.

data transferred here (only when valid & ready both asserted).

Exercise 2:



The diagram above shows a transfer over an SPI bus. How many bits of data are transferred? What is the value, in decimal, of the data transferred from the master to the slave? From the slave to the master?

8 bits transferred (8 rising edges of SCLK while asserted).

MOSI: (to slave)

8'b1100 0100

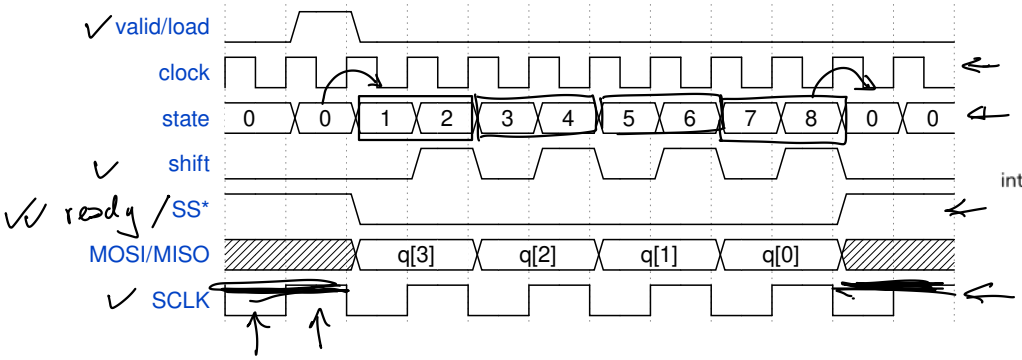
= 8'd 196

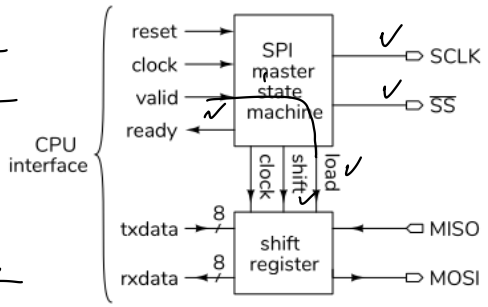
MISO: (to master)

8'b 0100 1011

= 8'd 75

Exercise 3:





Based on the diagram above, write a state transition table for an SPI interface controller that transfers four bits at a time. Include an idle state. In which states are **SCLK** and $\overline{\text{SS}}$ asserted?

State	SCLK	SS_n
0000		
0001		
;		
;		
1000		

```
logic state [3:0];
assign sclk = !state[0];
assign ss_n = state == 0;
assign load = valid;
assign shift = state == 2
              || state == 4 || ... ;
assign ready = ss_n;
always_ff @(posedge clk)
  state <= reset ? '0 :
           load & valid ? 1 :
           state == 8 ? 0 :
           state + 1 ;
```