More Verilog

active low

Exercise 1: Is a signal named **overload** active-high or active-low? Is there an overload if this signal is high? What if the signal was named **overload**?

overload is active low

H → false

overload → active high

H → true

Exercise 2: Come up with active-high and an active-low names for a signal that is at 3 V when a door is open and 0 V when the door is closed.

3V → open

0V → closed

active high: open

active low: closed

not: open → active low

low → open. X

Exercise 3: If **D** is a word and **D[0]** is low, is the word an even or odd number?

H → 1

L → 0

D[7:0] – 8 bit number

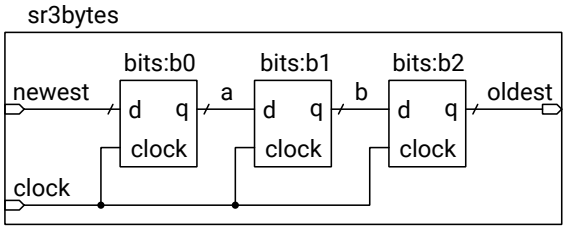
D: 00...001 → LLLL...LH

D: 000...01 → HHH... HL

D[0]

l.s. bit is 1 so it is an odd number.

Exercise 4:

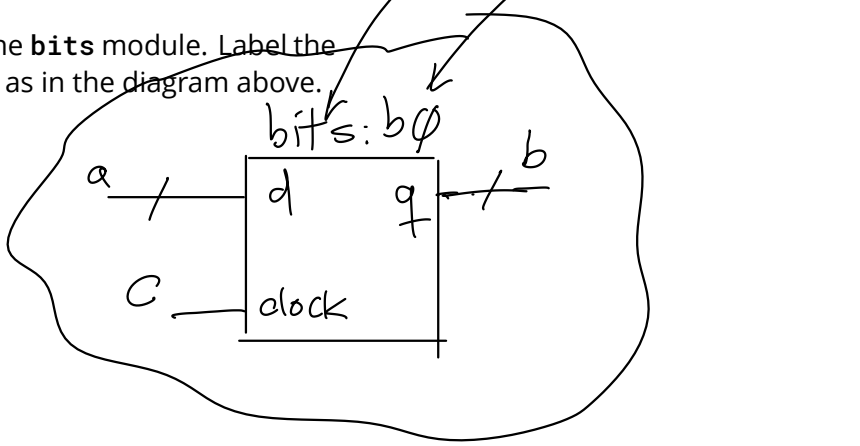


Draw a diagram for this instantiation of the **bits** module. Label the module, instance, signal and port names as in the diagram above.

```
bits #(4) b0 (a,b,c) ;
```

a, b, c are signals

d, q, clock are ports.



Exercise 5:

```
module sr3bytes
   (
    input  logic [7:0] newest,
    output logic [7:0] oldest,
    input  logic clock
    ) ;

   localparam nbits = 8 ;

   logic [nbits-1:0] a, b ;

   // matching by order
   bits #(nbits) b0 (newest,a,clock);

   // matching by name (order does not matter)
   bits #(.nb(nbits)) b1 (.q(b),.clock,.d(a));

   // wildcards for names that match
   bits #(.nb(nbits)) b2 (.d(b),.q(oldest),.*);

endmodule
```

instantiations

Identify the module instantiation statements in the code above. For each one, what is the instantiated module's name? The instance name?

→ bits

b0
b1
b2