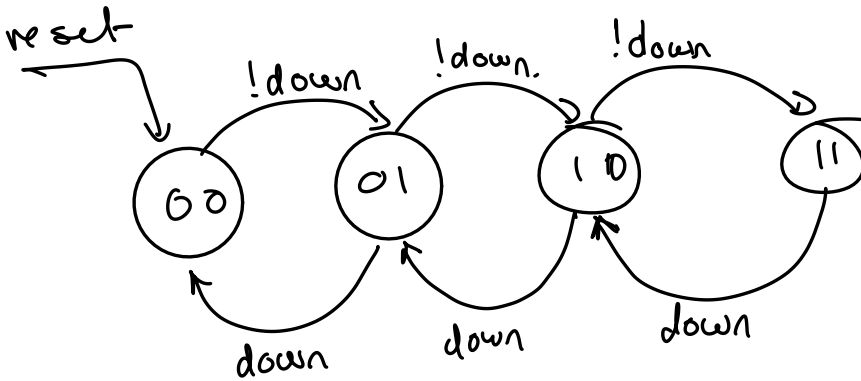
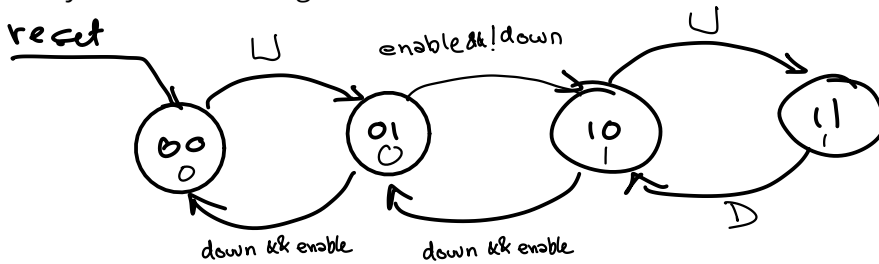


# State Machines

**Exercise 1:** Modify the diagram so the state machine counts to 11 and stops. Add a "down" input that cause the values to count down.



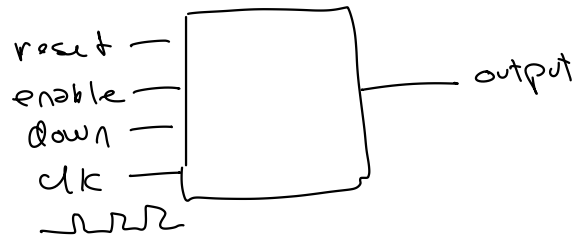
**Exercise 2:** Show the state transition diagram and table for a 2-bit counter with reset, enable, and down inputs. Reset should have priority. Write the Verilog.



$D \equiv \text{down} \&\& \text{enable}$   
 $U \equiv \text{!down} \&\& \text{enable}$

current state	reset	enable	down	next state	
X X	1	X	X	00	✓
00	0	0	X	00	
01	0	0	X	01	
00	0	1	1	01	✓
01	0	1	1	00	✓
01	0	1	0	10	✓
10	0	1	1	01	✓
10	0	1	0	11	✓
11	0	1	1	10	✓
11	0	1	0	11	✓

state	output
00	0
01	0
10	1
11	1



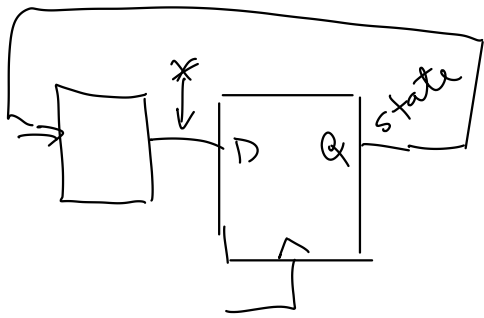
always\_ff @(posedge clk)  
 state <= reset ?

current state	reset	enable	down	next state
X X	1	X	X	00
00	0	0	X	00
00	0	1	0	01
01		1	1	00
		1	0	10
10		1	1	01
		1	0	11
11		1	1	10
		1	0	11

always\_ff @(posedge clk)  
state <= reset ? 2'b00 :  
!enable ? state :

state == 2'b00 && !down ? 2'b01 :  
state == 2'b01 && down ? 2'b00 :  
state == 2'b01 && !down ? 2'b10 :  
state == 2'b10 && down ? 2'b01 :  
state == 2'b10 && !down ? 2'b11 :  
state == 2'b11 && down ? 2'b10 :  
state ;

*could combine*

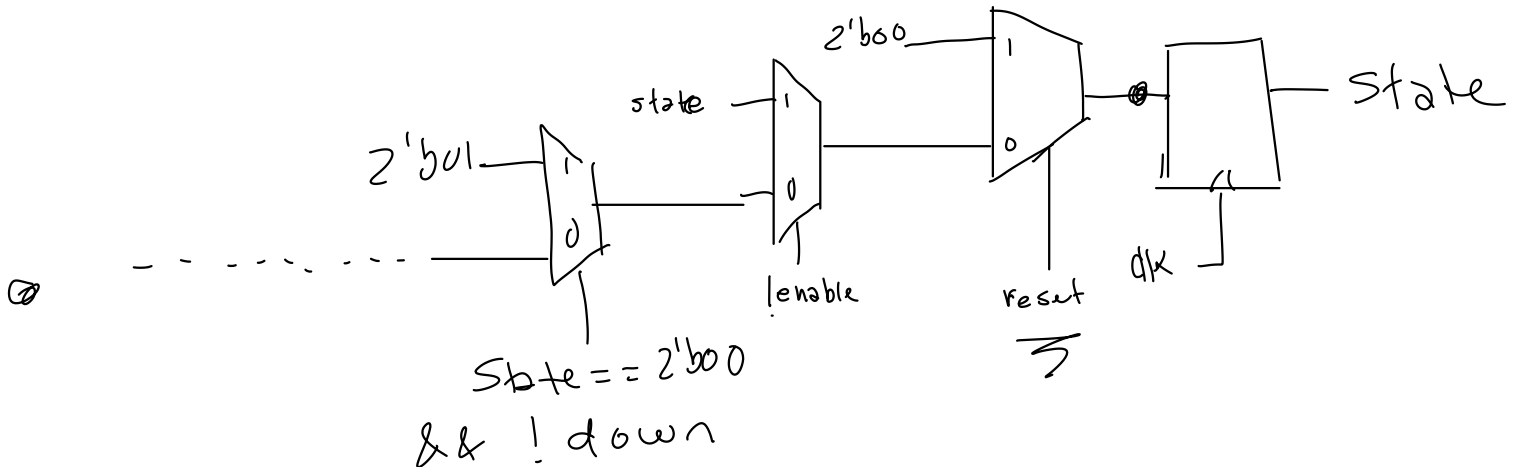


assign output = state == 2'b10 ||  
state == 2'b11 ? 1'b1 : 1'b0;

or  
= state == 2'b10 ||  
state == 2'b11 ;

always\_ff @(..)  
state <= \*

Exercise 2b (3): Draw the schematic:





**Exercise 3:** What value of  $N$  would result in a 20 ms delay if the clock frequency is 50 MHz? How many bits are needed for this timer's register?

$$N = ? \quad NT = \frac{20 \times 10^{-3}}{f} \quad f = 50 \times 10^6$$

$$T = \frac{1}{f} = \frac{1}{50 \times 10^6} = \frac{1}{.05 \times 10^9} = 20 \times 10^{-9} = 20 \text{ ns.}$$

$$N = \frac{NT}{T} = \frac{20 \times 10^{-3}}{20 \times 10^{-9}} = 1 \times 10^6$$

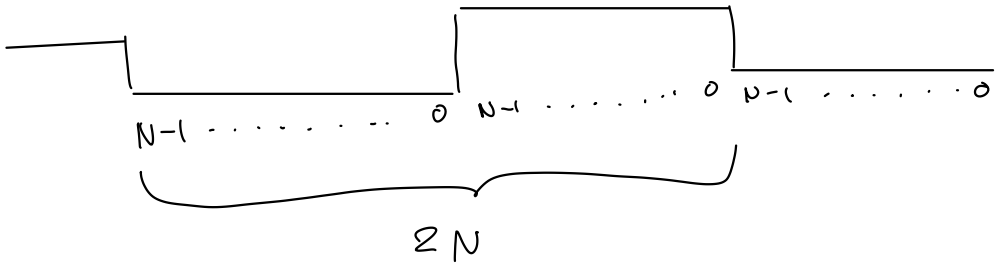
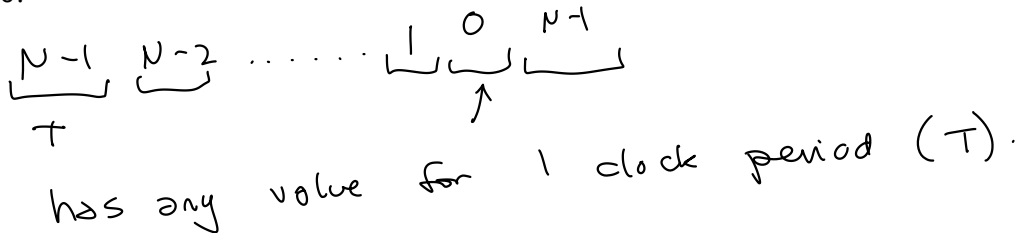
$$2^{20} = 1024 \cdot 1024 = 2^{20} \approx 10^6$$

$$\log_2 2^n \geq \log_2 10^6$$

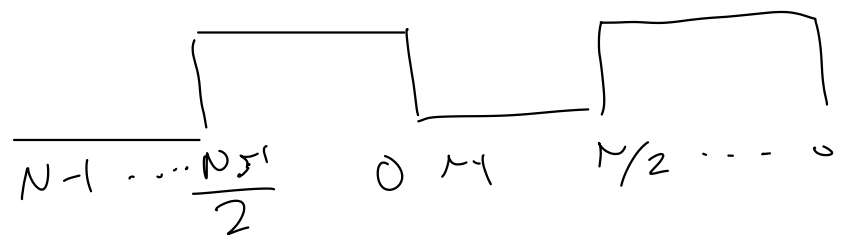
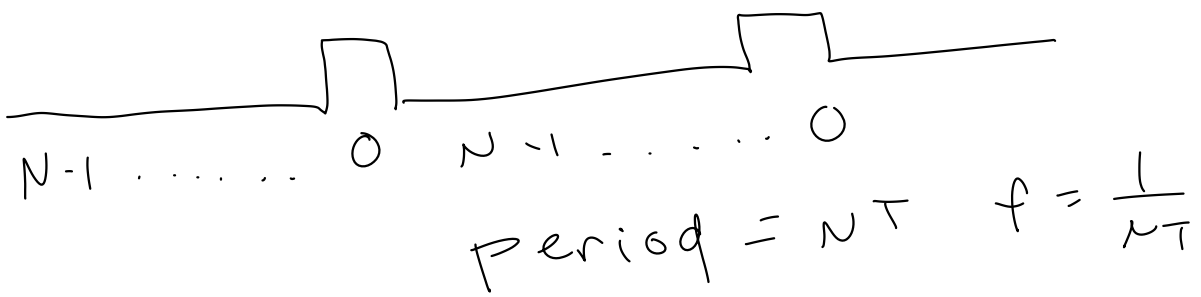
$$n \geq 19.9 \dots$$

use 20 bits

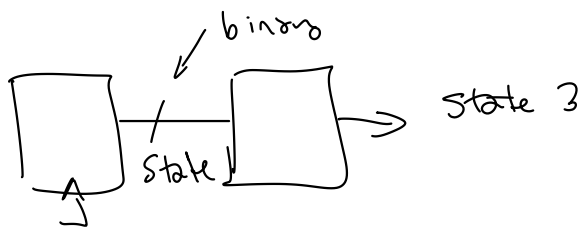
**Exercise 4:** Assume the timer above is reset to  $N - 1$  each time it reaches 0. For how long is the register value 0? What are the period and frequency of a signal that is inverted each time the count reaches 0?



period =  $2NT$       freq =  $\frac{1}{2NT}$



**Exercise 5:** How many bits are need to be to detect a state when a binary encoding is used? With a one-hot encoding?



- binary encoding: need all bits
- one-hot: only one bit.

**Exercise 6:** If we used 8-bits of state information, how many states could be represented? What if we used 8 bits of state but used a "one-hot" encoding?

- w/ binary encoding we can have  $0 \dots 2^8 = 0 \dots 255$   
256 different states.
- w/ one-hot 1000 0000, 0100 0000,  $\dots$  0000 0001