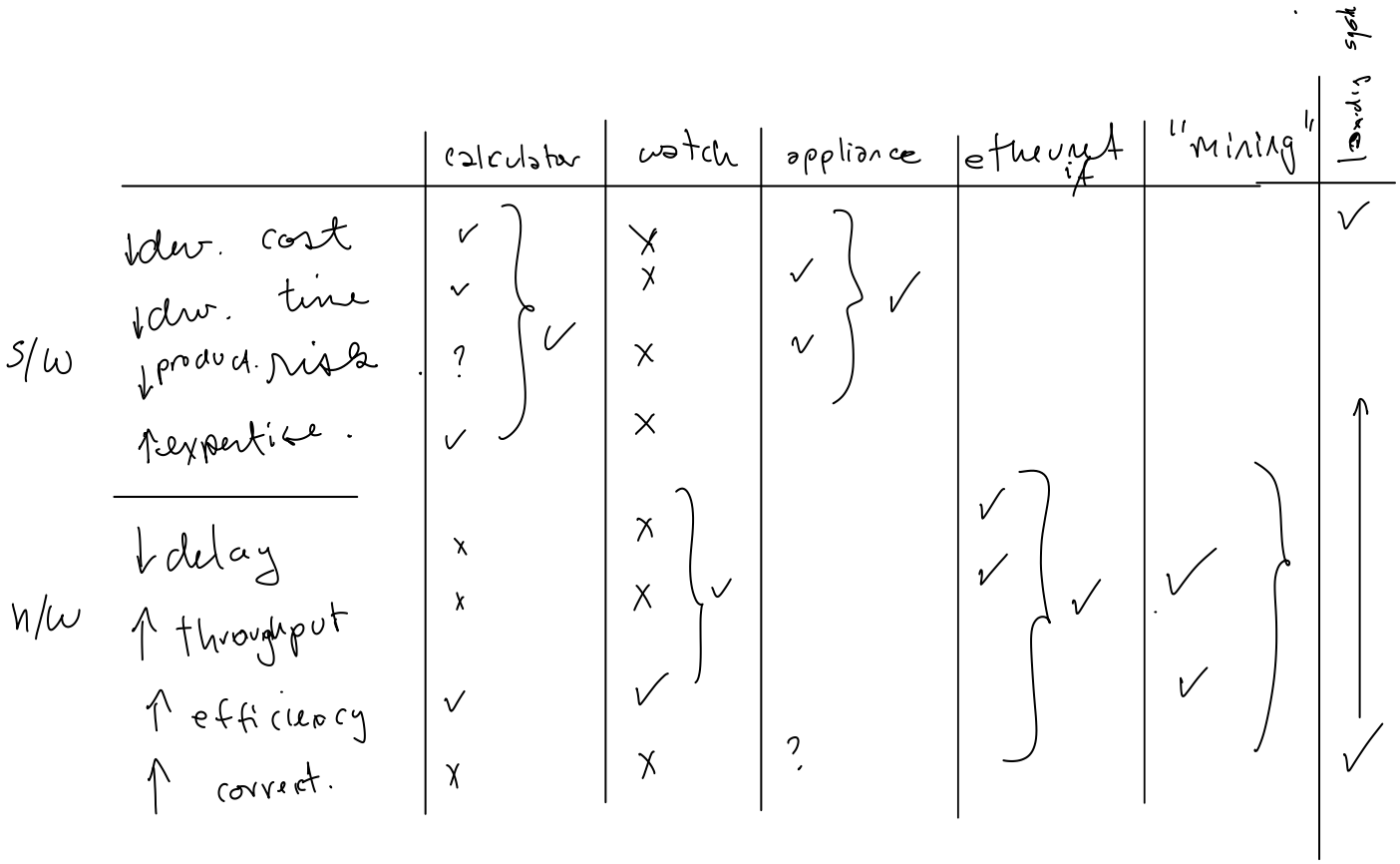
Programmable Logic Applications and Architectures

Exercise 1: Would you use hardware or software to implement: A new calculator? A digital watch? A controller for a kitchen appliance? An Ethernet interface? For Cryptocurrency "mining"? For an aircraft's automated landing system?

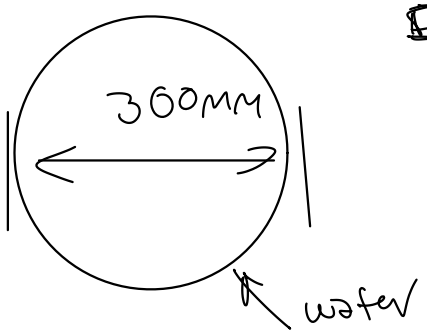


Exercise 2: What improvement in number of transistors per unit area would be achieved by reducing the feature size from 7 nm to 5 nm? Approximately how many 5x5 mm die fit on a 300 mm wafer? How many 200x200 nm gates fit on the die?

7nm → area. 7 □ = 49 sq nm.

5nm → 5 □ = 25 sq nm.

transistors/area = 1/49 vs 1/25 ≈ 2x increase in #/area.



$$\approx \frac{2\pi r^2}{5\times 5} = 5600 \text{ die.}$$

Exercise 3: Would you use a PLD or ASIC for: A project that had to be completed within a month? That would be expected to sell 100 million units? Whose complete requirements aren't known? A state-of-the-art general-purpose CPU?

1 month TTM: FPGA

100 million volume: ASIC

uncertain reqmnts: FPGA

high performance: ASIC.