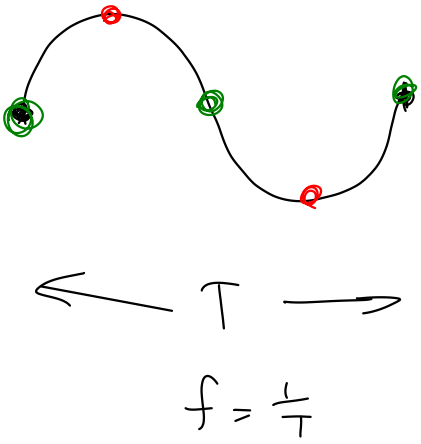
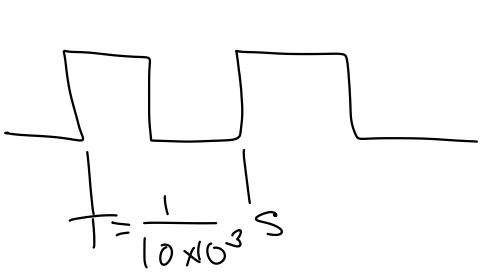
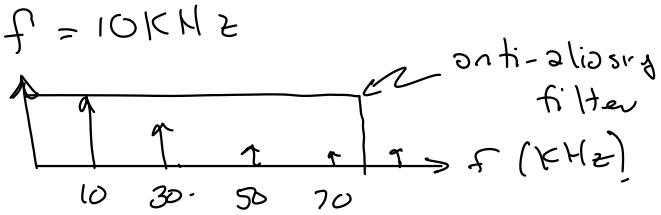
Analog Interfaces

Exercise 1: Draw a sine wave and indicate two sets of sampling points at twice the frequency of the sine wave: one that demonstrates aliasing and one that does not. Is it sufficient to sample at twice the highest frequency of the analog signal?



Exercise 2: What minimum sampling rate would be required to digitize a 10 kHz square wave if you wanted to include frequency components up to the 7'th harmonic (at 70 kHz)?

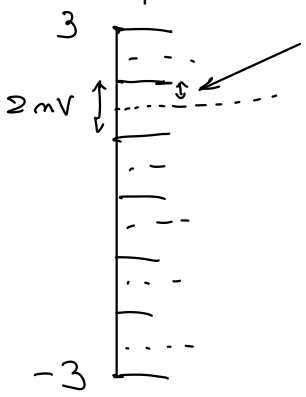




sampling freq > 2 x 70 kHz

> 140 kHz.

Exercise 3: A signal with range of ± 3 V must be quantized so that the quantization error is less than 1 mV. What minimum number of bits of resolution is required?



1mV (max quantization error)

number quantization levels $= \frac{3-(-3)\,V}{2\,mV}$

$= \frac{6}{.002} = 3000$

We want # step to be a power of 2

$2^n \geq 3000$

$\log_2 2^n = n \geq \log_2 3000$

$n \geq 11.55$

use $n = 12$ bits

for $n = 12$

step size (resolution)

$= \frac{6}{4096} \approx 1.5\,mV.$

Exercise 4: A signal-to-noise power ratio of about 48 dB is considered "good enough" for speech communication. Approximately how many bits per sample are required to obtain this quantization SNR?

Assuming we can use the quant. SNR formula for sinewaves,

$$SNR \approx 2 + 6n \ (dB)$$

$$\geq 48$$

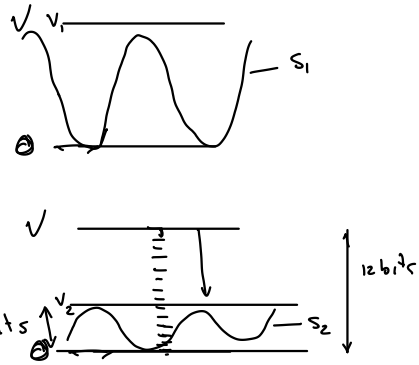
$$2 + 6n \geq 48$$

$$6n \geq 46$$

$$n \geq \frac{46}{6} = 7.6$$

use $n = 8$ bits

Exercise 5: When quantizing a full-scale sine wave, what quantization SNR would be achieved with a resolution of 12 bits? What if the signal's voltage range was only half of the full-scale range?



$$QSNR = 1.76 + 6n \text{ dB}$$
$$= 1.76 + 6 \cdot 12$$
$$= 73.76 \text{ dB}$$

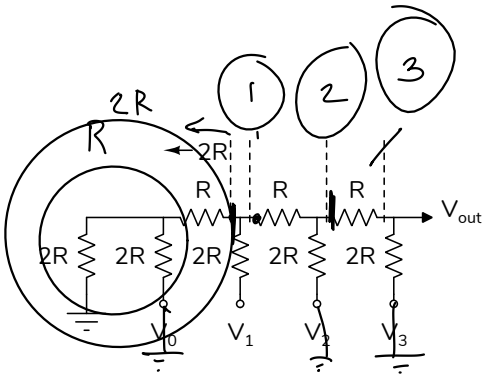
if use only half the range
then only 1/2 number of steps (1 bit less resolution).

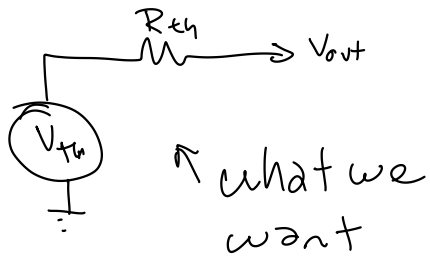
$$QSNR = 1.76 + 6 \cdot 11$$
$$= 67.76.$$

$\frac{S}{N} \rightarrow$

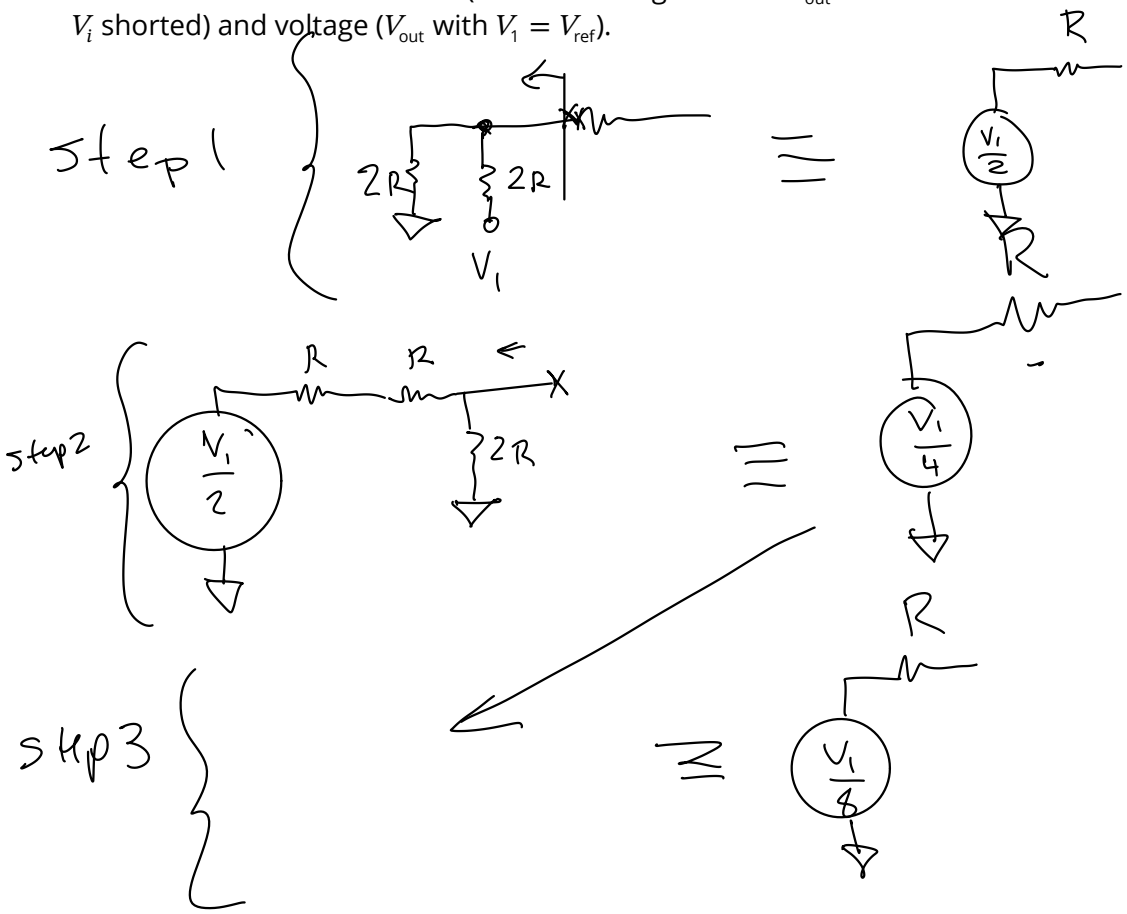
$$\text{change in } S = 10\log\left(\frac{S_2}{S_1}\right)$$
$$= 10\log\left(\frac{(V_1/2)^2}{V_1^2}\right)$$
$$= 20\log\left(\frac{1}{2}\right)$$
$$= -6\text{dB}.$$

Exercise 6:

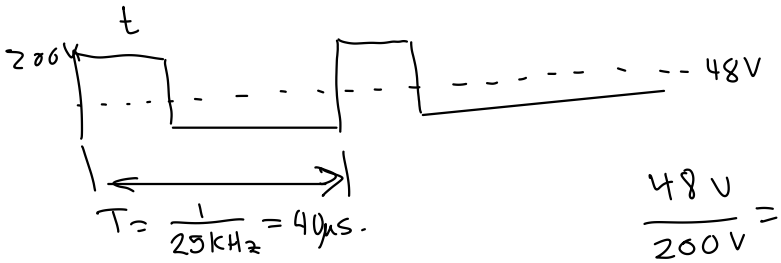




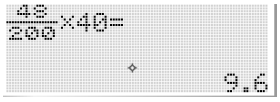
Assume V_1 is set to V_{ref} and all other inputs are zero (grounded). Find the Thevenim resistance (resistance to ground at V_{out} with all V_i shorted) and voltage (V_{out} with $V_1 = V_{ref}$).



Exercise 7: You are using a PWM DAC to convert a 200 VDC supply to a 48 VDC output. The switching frequency is 25 kHz. What is the duration of each PWM pulse?

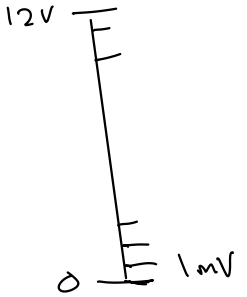


$$\frac{48\,V}{200\,V} = \frac{t}{T}$$



$$t = \frac{48}{200} \cdot 40\mu s = 9.6\mu s$$

Exercise 8: You are designing a PWM DAC and need resolution of 1 mV with a full-scale output of 12 V. How many bits of resolution are required? The pulse frequency is 10 kHz. What is the clock frequency?



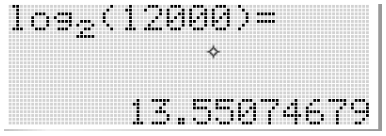
resolution = 1mV

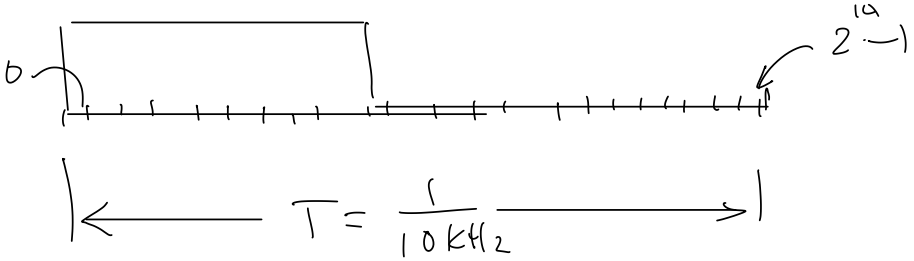
resolution = n bits

steps = 12,000

need $\log_2 12000$ bits

$n = 13.5$ (use 14 bits)





$\approx 100\,\mu s$.

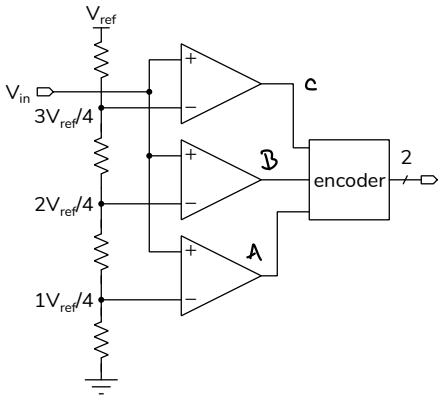
clock frequency is $2^{14} \cdot 10\,kHz \approx 163\,MHz$

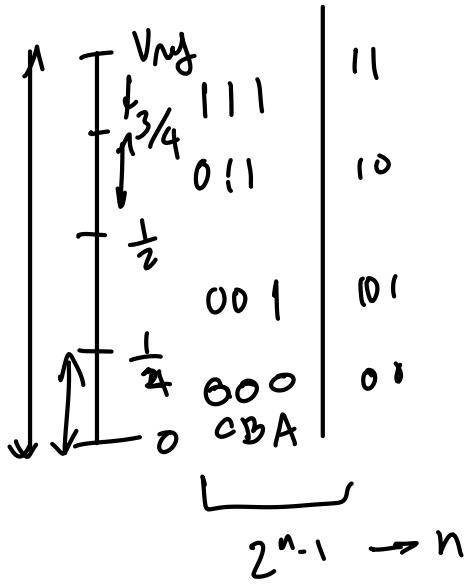
16,384.

Exercise 9: Rank the different DACs described above in terms of sampling rate relative to clock rate and complexity relative to resolution.

	clocks/output	analog complexity
binary weighted (R-2R)	1	n resistors/bit.
PWM	2^n	small
$\Sigma\Delta$	$\ll 2^n$	smaller.

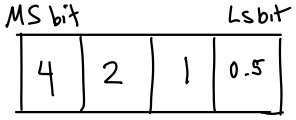
Exercise 10:





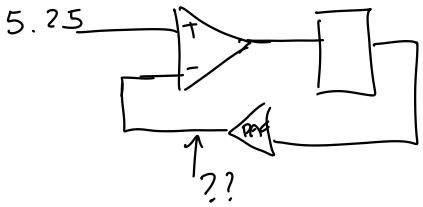
Draw a diagram showing the voltage ranges, the comparator outputs and the binary output for the 4-bit flash ADC above.

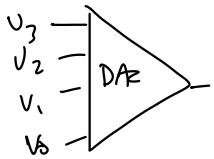
Exercise 11: A SAR ADC using a 4-bit DAC with a full-scale range of 0 to 7.5 V digitizes a 5.25 V signal. What voltages will the DAC output?



0000 → 0 each step is 0.5V.

1111 → 7.5V



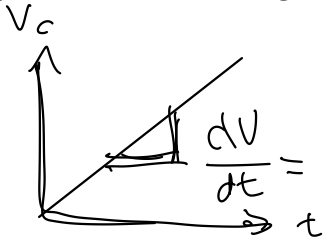


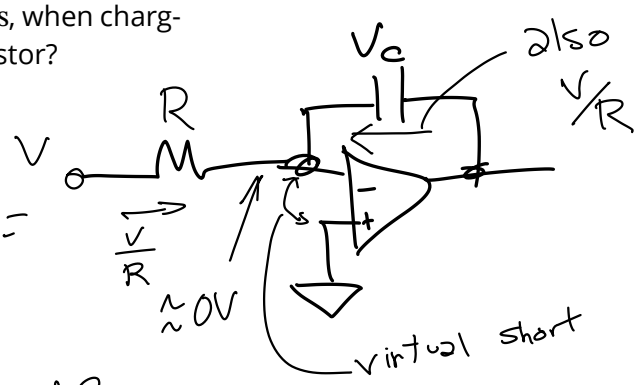
comparator

DAC i/p	DAC o/p (V)	
1000	→ 4	→ 1
1100	→ 6	→ 0
1010	→ 5	→ 1
1011	→ 5.5	→ 0

1010

Exercise 12: What is the slope of an integrator, in V/s, when charging a 100 nF capacitor with 5 V through a 100 kΩ resistor?

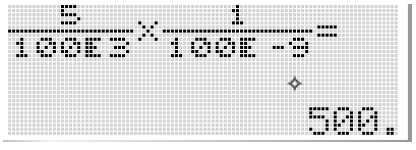




from $Q = CV \rightarrow V = \frac{Q}{C}$ $\quad i_c = \frac{dQ}{dt}$

$$\frac{dV}{dt} = \frac{dQ}{dt}\frac{1}{C} = \frac{i_c}{C} = \frac{V/R}{C} = \frac{5\,V/106\times10^{3}\,\Omega}{100\times10^{-9}\,F}$$

$$= 500\ V/s$$



check units: $F = \frac{C}{V}$ $\quad A = \frac{C}{s}$ $\quad \frac{A}{F} = \frac{V}{s}$

Exercise 13: Rank the different ADCs described above in terms of sampling rate relative to clock rate and complexity relative to resolution.

	clock cycle/sample	complexity
flash	1	2^n comparator
SAR	n	(1 comparator) n-bit DAC
$\Sigma\Delta$	100 (depends)	1 comparator + LPF
dual-slope	2^n	1 comparator + 1 integrator.